REJ03B0171-0110
Rev.1.10
Oct. 31, 2005

1. Overview

The M32C/88 Group (M32C/88T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 Series CPU core. The M32C/88 Group (M32C/88T) is available in 144-pin and 100-pin plastic molded LQFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.2 Performance Overview

Tables 1.1 and 1.2 list performance overview of the M32C/88 Group (M32C/88T).

Table 1.1 M32C/88 Group (M32C/88T) Performance (144-Pin Package)

Characteristic		Performance
CPU	Basic Instructions	108 instructions
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, VCC=4.2 V to 5.5 V)
	Operating Mode	Single-chip mode
	Address Space	16 Mbytes
	Memory Capacity	See Table 1.3
Peripheral Function	I/O Port	123 I/O pins and 1 input pin
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I2C bus(2)
	CAN Module	3 channels Supporting CAN 2.0B specification
	A/D Converter	10-bit A/D converter: 1 circuit, 34 channels
	D/A Converter	8 bits x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions
	CRC Calculation Circuit	CRC-CCITT
	X/Y Converter	16 bits x 16 bits
	Watchdog Timer	15 bits x 1 channel (with prescaler)
	Interrupt	40 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally
	Oscillation Stop Detect Function	Main clock oscillation stop detect function
	Cold Start-up/Warm Start-up Determine Function	On-chip (option)
Electrical Characteristics	Supply Voltage	VCC=4.2 V to 5.5 V, (f(BCLK)=32 MHz)
	Power Consumption	28 mA (VCC=5 V, f(BCLK)=32 MHz) 10µA (VCC=5 V, f(BCLK)=32 kHz, in wait mode)
Flash Memory	Program/Erase Supply Voltage	5.0 V ± 0.5 V
	Program and Erase Endurance	100 times (all space)
Operating Ambient Temperature		–40 to 85°C (T version) –40 to 105°C (U version)
Package		144-pin plastic molded LQFP

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
2. I2C bus is a trademark of Koninklijke Philips Electronics N. V.

All options are on a request basis.

Table 1.2 M32C/88 Group (M32C/88T) Performance (100-Pin Package)

Characteristic		Performance
CPU	Basic Instructions	108 instructions
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, VCC=4.2 V to 5.5 V)
	Operating Mode	Single-chip mode
	Address Space	16 Mbytes
	Memory Capacity	See Table 1.3
Peripheral Function	I/O Port	87 I/O pins and 1 input pin
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I2C bus(2)
	CAN Module	3 channels Supporting CAN 2.0B specification
	A/D Converter	10-bit A/D converter: 1 circuit, 34 channels
	D/A Converter	8 bits x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions
	CRC Calculation Circuit	CRC-CCITT
	X/Y Converter	16 bits x 16 bits
	Watchdog Timer	15 bits x 1 channel (with prescaler)
	Interrupt	40 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally
	Oscillation Stop Detect Function	Main clock oscillation stop detect function
	Cold Start-up/Warm Start-up Determine Function	On-chip (option)
Electrical Characteristics	Supply Voltage	VCC=4.2 V to 5.5 V, (f(BCLK)=32 MHz)
	Power Consumption	28 mA (VCC=5 V, f(BCLK)=32 MHz) 10µA (VCC=5 V, f(BCLK)=32 kHz, in wait mode)
Flash Memory	Program/Erase Supply Voltage	5.0 V ± 0.5 V
	Program and Erase Endurance	100 times (all space)
Operating Ambient Temperature		–40 to 85°C (T version) –40 to 105°C (U version)
Package		100-pin plastic molded LQFP

NOTES:

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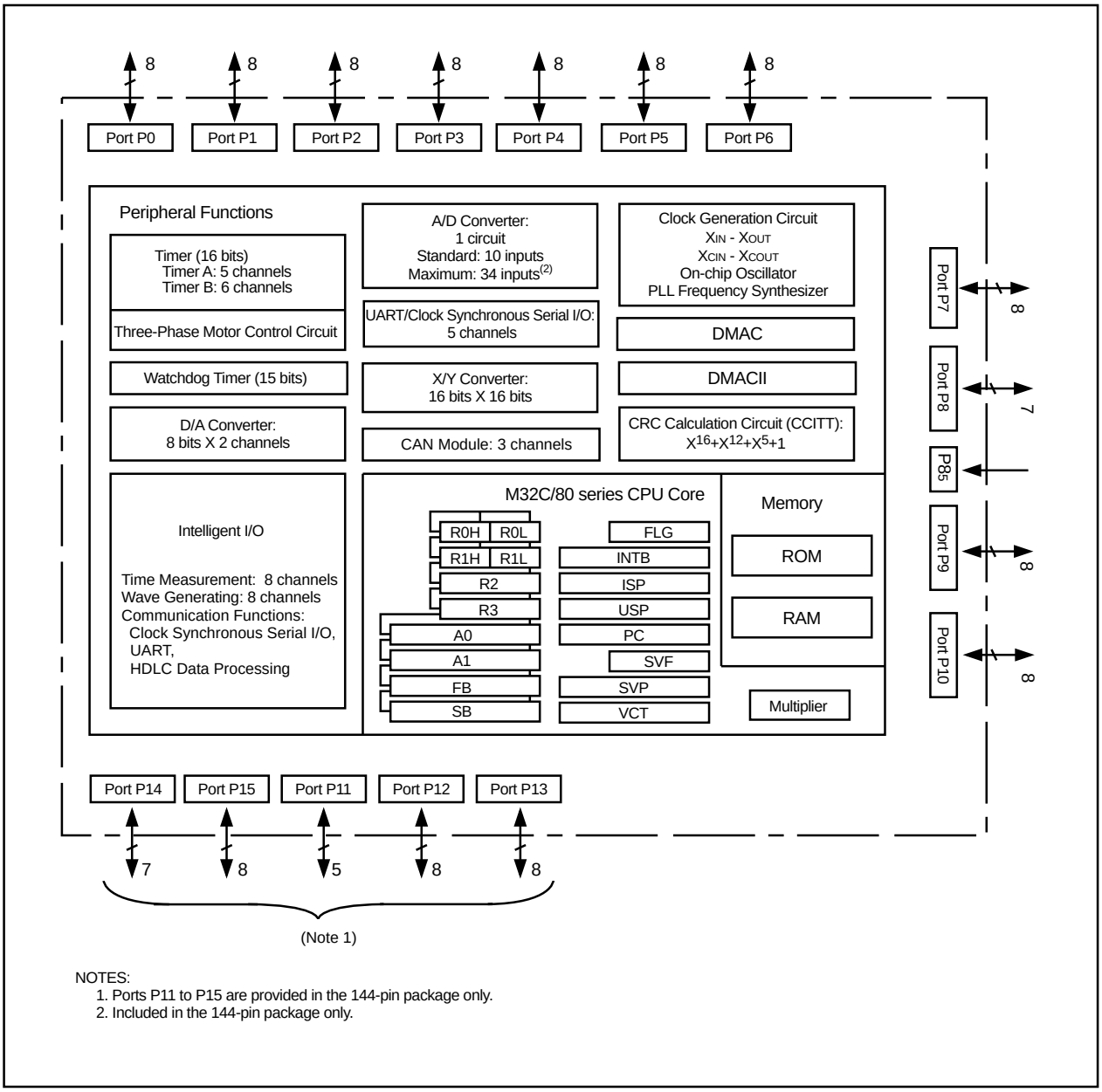
2. I2C bus is a trademark of Koninklijke Philips Electronics N. V.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/88 Group (M32C/88T) microcomputer.



NOTES:
1. Ports P11 to P15 are provided in the 144-pin package only.
2. Included in the 144-pin package only.

Figure 1.1 M32C/88 Group (M32C/88T) Block Diagram

1.4 Product Information

Table 1.3 lists the product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/88 Group (1) (T version, M32C/88T) **As of October, 2005**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30882FJTGP (D)	PLQP0144KA-A (144P6Q-A)	512K+4K	18K	Flash Memory T version (High-reliability 85° C)
M30880FJTGP (D)	PLQP0100KB-A (100P6Q-A)			
M30882FHTGP (D)	PLQP0144KA-A (144P6Q-A)	384K+4K		
M30880FHTGP (D)	PLQP0100KB-A (100P6Q-A)			
M30882FWTGP (D)	PLQP0144KA-A (144P6Q-A)	320K+4K		
M30880FWTGP (D)	PLQP0100KB-A (100P6Q-A)			

(D): Under development

Table 1.3 M32C/88 Group (2) (U version, M32C/88T) **As of October, 2005**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30882FJUGP (D)	PLQP0144KA-A (144P6Q-A)	512K+4K	18K	Flash Memory U version (High-reliability 105° C)
M30880FJUGP (D)	PLQP0100KB-A (100P6Q-A)			
M30882FHUGP (D)	PLQP0144KA-A (144P6Q-A)	384K+4K		
M30880FHUGP (D)	PLQP0100KB-A (100P6Q-A)			
M30882FWUGP (D)	PLQP0144KA-A (144P6Q-A)	320K+4K		
M30880FWUGP (D)	PLQP0100KB-A (100P6Q-A)			

(D): Under development

NOTE:

Contact our sales office if you are interested in the V version.

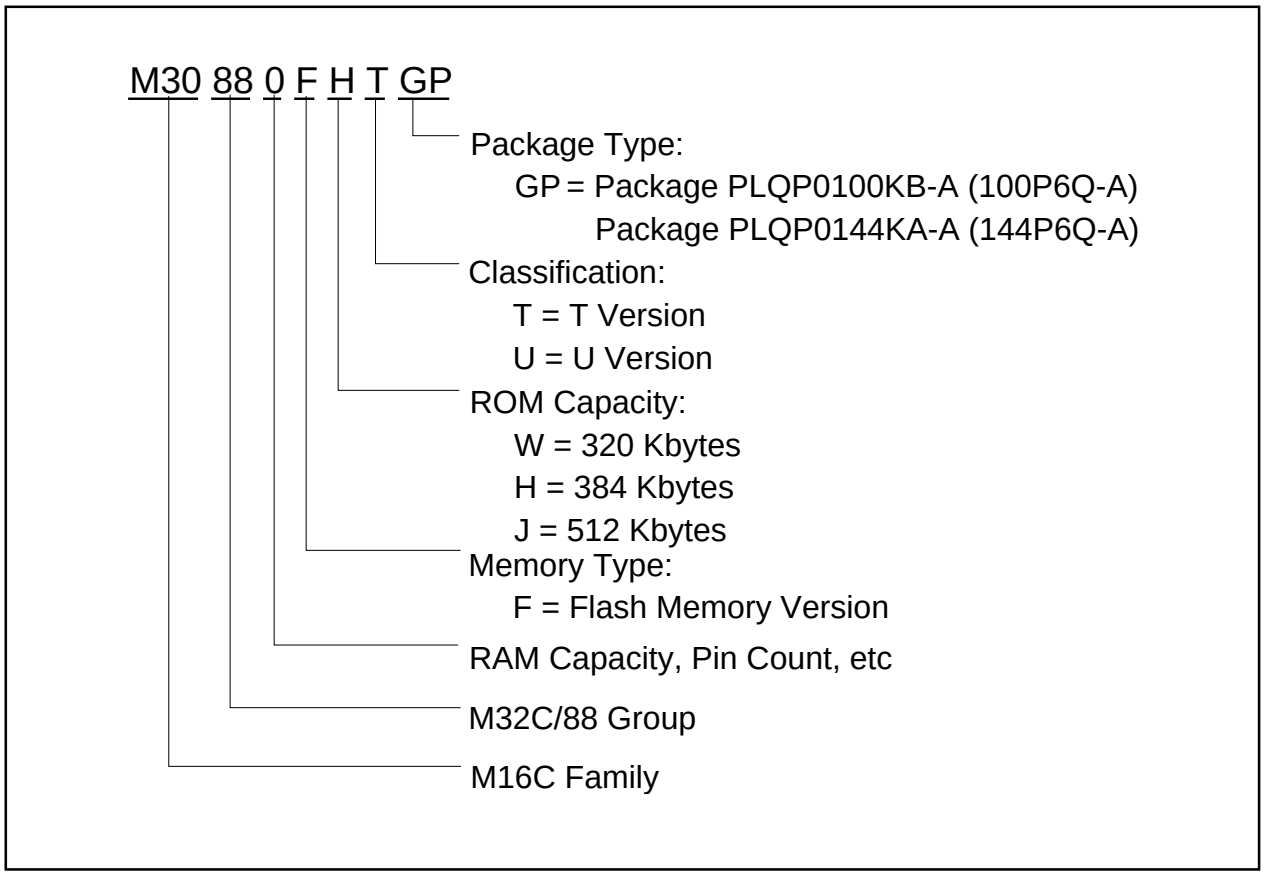


Figure 1.2 Product Numbering System

1.5 Pin Assignment

Figures 1.3 and 1.4 show pin assignments (top view).

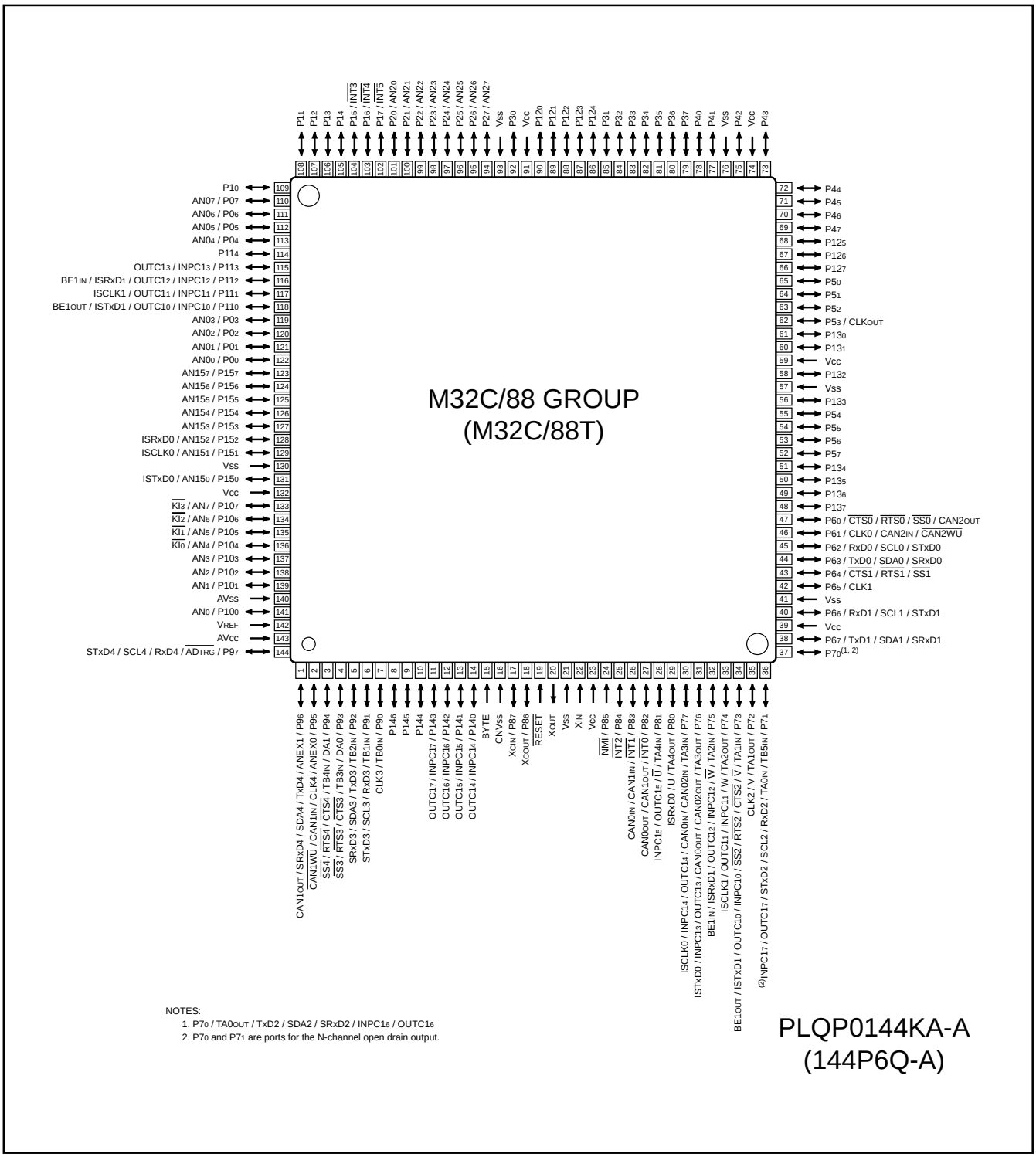


Figure 1.3 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin
1		P9$_6$			TxD4/SDA4/SRxD4/CAN1$_{OUT}$		ANEX1
2		P9$_5$			CLK4/CAN1$_{IN}$/$\overline{CAN1WU}$		ANEX0
3		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1
4		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0
5		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3		
6		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3		
7		P9$_0$		TB0$_{IN}$	CLK3		
8		P14$_6$					
9		P14$_5$					
10		P14$_4$					
11		P14$_3$				INPC17/OUTC17	
12		P14$_2$				INPC16/OUTC16	
13		P14$_1$				INPC15/OUTC15	
14		P14$_0$				INPC14/OUTC14	
15	BYTE						
16	CNV$_{SS}$						
17	X$_{CIN}$	P8$_7$					
18	X$_{COUT}$	P8$_6$					
19	$\overline{RESET}$						
20	X$_{OUT}$						
21	V$_{SS}$						
22	X$_{IN}$						
23	V$_{CC}$						
24		P8$_5$	$\overline{NMI}$				
25		P8$_4$	$\overline{INT2}$				
26		P8$_3$	$\overline{INT1}$		CAN0$_{IN}$/CAN1$_{IN}$		
27		P8$_2$	$\overline{INT0}$		CAN0$_{OUT}$/CAN1$_{OUT}$		
28		P8$_1$		TA4$_{IN}$/$\overline{U}$		INPC15/OUTC15	
29		P8$_0$		TA4$_{OUT}$/U		ISRxD0	
30		P7$_7$		TA3$_{IN}$	CAN0$_{IN}$/CAN02$_{IN}$	INPC14/OUTC14/ISCLK0	
31		P7$_6$		TA3$_{OUT}$	CAN0$_{OUT}$/CAN02$_{OUT}$	INPC13/OUTC13/ISTxD0	
32		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC12/OUTC12/ISRxD1/BE1$_{IN}$	
33		P7$_4$		TA2$_{OUT}$/W		INPC11/OUTC11/ISCLK1	
34		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	INPC10/OUTC10/ISTxD1/BE1$_{OUT}$	
35		P7$_2$		TA1$_{OUT}$/V	CLK2		
36		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	INPC17/OUTC17	
37		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	INPC16/OUTC16	
38	V$_{CC}$	P6$_7$			TxD1/SDA1/SRxD1		
39	V$_{SS}$						
40		P6$_6$			RxD1/SCL1/STxD1		
41							
42		P6$_5$			CLK1		
43		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$		
44		P6$_3$			TxD0/SDA0/SRxD0		
45		P6$_2$			RxD0/SCL0/STxD0		
46		P6$_1$			CLK0/CAN2$_{IN}$/$\overline{CAN2WU}$		
47		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$/CAN2$_{OUT}$		
48		P13$_7$					

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin
49		$P13_6$					
50		$P13_5$					
51		$P13_4$					
52		$P5_7$					
53		$P5_6$					
54		$P5_5$					
55		$P5_4$					
56		$P13_3$					
57	V_{SS}						
58		$P13_2$					
59	V_{CC}						
60		$P13_1$					
61		$P13_0$					
62		$P5_3$					
63		$P5_2$					
64		$P5_1$					
65		$P5_0$					
66		$P12_7$					
67		$P12_6$					
68		$P12_5$					
69		$P4_7$					
70		$P4_6$					
71		$P4_5$					
72		$P4_4$					
73	V_{CC}	$P4_3$					
74							
75	V_{SS}	$P4_2$					
76							
77		$P4_1$					
78		$P4_0$					
79		$P3_7$					
80		$P3_6$					
81		$P3_5$					
82		$P3_4$					
83		$P3_3$					
84		$P3_2$					
85		$P3_1$					
86		$P12_4$					
87		$P12_3$					
88		$P12_2$					
89		$P12_1$					
90	V_{CC}	$P12_0$					
91	V_{SS}						
92		$P3_0$					
93							
94		$P2_7$					$AN2_7$
95		$P2_6$					$AN2_6$
96		$P2_5$					$AN2_5$

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin
97		$P2_4$					$AN2_4$
98		$P2_3$					$AN2_3$
99		$P2_2$					$AN2_2$
100		$P2_1$					$AN2_1$
101		$P2_0$					$AN2_0$
102		$P1_7$	$\overline{INT5}$				
103		$P1_6$	$\overline{INT4}$				
104		$P1_5$	$\overline{INT3}$				
105		$P1_4$					
106		$P1_3$					
107		$P1_2$					
108		$P1_1$					
109		$P1_0$					
110		$P0_7$					$AN0_7$
111		$P0_6$					$AN0_6$
112		$P0_5$					$AN0_5$
113		$P0_4$					$AN0_4$
114		$P11_4$					
115		$P11_3$				$INPC1_3$/$OUTC1_3$	
116		$P11_2$				$INPC1_2$/$OUTC1_2$/ISRxD1/$BE1_{IN}$	
117		$P11_1$				$INPC1_1$/$OUTC1_1$/ISCLK1	
118		$P11_0$				$INPC1_0$/$OUTC1_0$/ISTxD1/$BE1_{OUT}$	
119		$P0_3$					$AN0_3$
120		$P0_2$					$AN0_2$
121		$P0_1$					$AN0_1$
122		$P0_0$					$AN0_0$
123		$P15_7$					$AN15_7$
124		$P15_6$					$AN15_6$
125		$P15_5$					$AN15_5$
126		$P15_4$					$AN15_4$
127		$P15_3$					$AN15_3$
128		$P15_2$				ISRxD0	$AN15_2$
129		$P15_1$				ISCLK0	$AN15_1$
130	V_{SS}						
131		$P15_0$				ISTxD0	$AN15_0$
132	V_{CC}						
133		$P10_7$	$\overline{KI_3}$				AN_7
134		$P10_6$	$\overline{KI_2}$				AN_6
135		$P10_5$	$\overline{KI_1}$				AN_5
136		$P10_4$	$\overline{KI_0}$				AN_4
137		$P10_3$					AN_3
138		$P10_2$					AN_2
139		$P10_1$					AN_1
140	AV_{SS}						
141		$P10_0$					AN_0
142	V_{REF}						
143	AV_{CC}						
144		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$

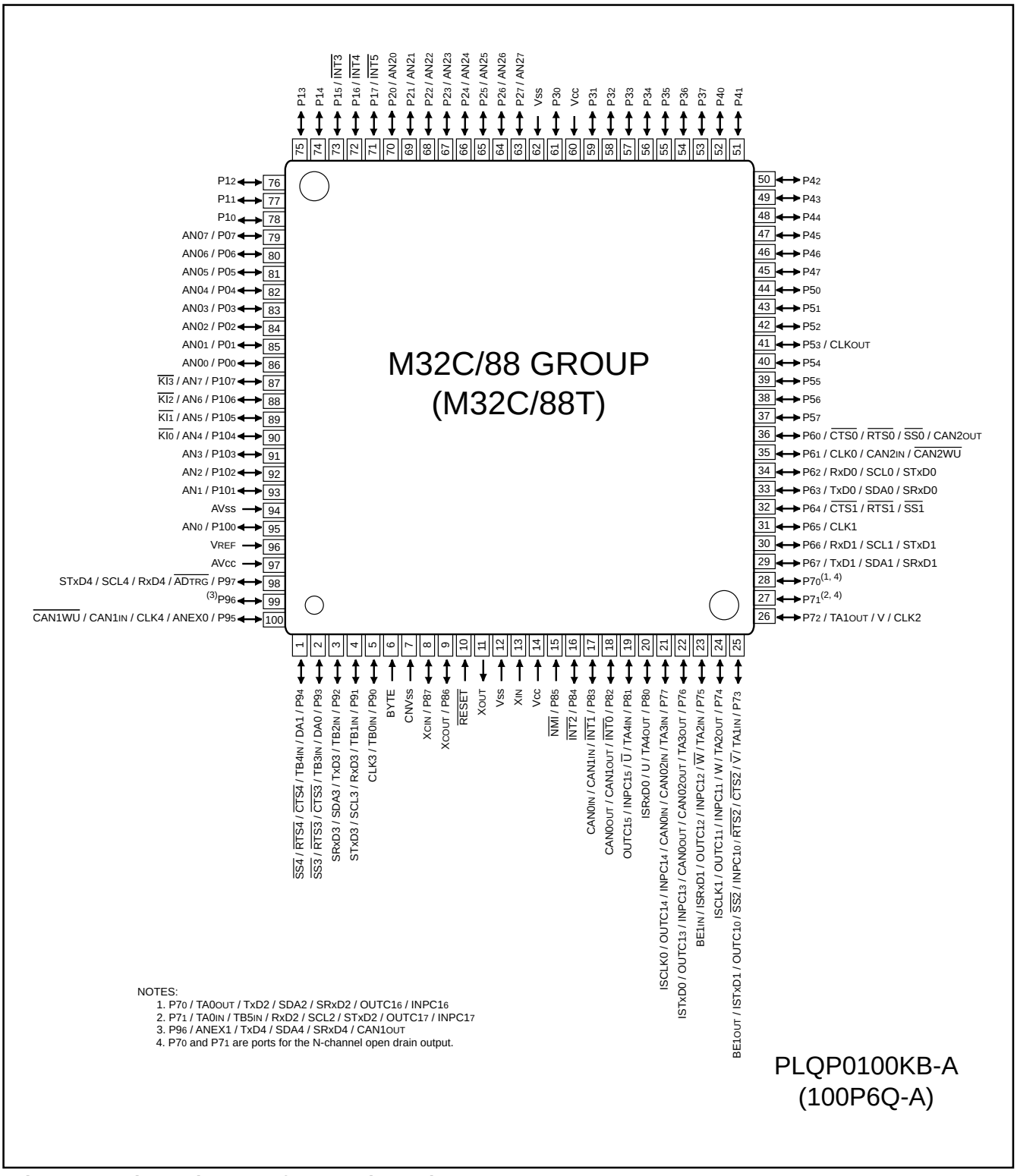


Figure 1.4 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin
1		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1
2		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0
3		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3		
4		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3		
5		P9$_0$		TB0$_{IN}$	CLK3		
6	BYTE						
7	CNV$_{SS}$						
8	X$_{CIN}$	P8$_7$					
9	X$_{COUT}$	P8$_6$					
10	$\overline{RESET}$						
11	X$_{OUT}$						
12	V$_{SS}$						
13	X$_{IN}$						
14	V$_{CC}$						
15		P8$_5$	$\overline{NMI}$				
16		P8$_4$	$\overline{INT2}$				
17		P8$_3$	$\overline{INT1}$		CAN0$_{IN}$/CAN1$_{IN}$		
18		P8$_2$	$\overline{INT0}$		CAN0$_{OUT}$/CAN1$_{OUT}$		
19		P8$_1$		TA4$_{IN}$/$\overline{U}$		INPC1$_5$/OUTC1$_5$	
20		P8$_0$		TA4$_{OUT}$/U		ISRxD0	
21		P7$_7$		TA3$_{IN}$	CAN0$_{IN}$/CAN02$_{IN}$	INPC1$_4$/OUTC1$_4$/ISCLK0	
22		P7$_6$		TA3$_{OUT}$	CAN0$_{OUT}$/CAN02$_{OUT}$	INPC1$_3$/OUTC1$_3$/ISTxD0	
23		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$	
24		P7$_4$		TA2$_{OUT}$/W		INPC1$_1$/OUTC1$_1$/ISCLK1	
25		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	INPC1$_0$/OUTC1$_0$/ISTxD1/BE1$_{OUT}$	
26		P7$_2$		TA1$_{OUT}$/V	CLK2		
27		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	INPC1$_7$/OUTC1$_7$	
28		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	INPC1$_6$/OUTC1$_6$	
29		P6$_7$			TxD1/SDA1/SRxD1		
30		P6$_6$			RxD1/SCL1/STxD1		
31		P6$_5$			CLK1		
32		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$		
33		P6$_3$			TxD0/SDA0/SRxD0		
34		P6$_2$			RxD0/SCL0/STxD0		
35		P6$_1$			CLK0/CAN2$_{IN}$/$\overline{CAN2WU}$		
36		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$/CAN2$_{OUT}$		
37		P5$_7$					
38		P5$_6$					
39		P5$_5$					
40		P5$_4$					
41		P5$_3$					
42		P5$_2$					
43		P5$_1$					
44		P5$_0$					
45		P4$_7$					
46		P4$_6$					
47		P4$_5$					
48		P4$_4$					
49		P4$_3$					
50		P4$_2$					

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin
51		$P4_1$					
52		$P4_0$					
53		$P3_7$					
54		$P3_6$					
55		$P3_5$					
56		$P3_4$					
57		$P3_3$					
58		$P3_2$					
59		$P3_1$					
60	V_{CC}						
61		$P3_0$					
62	V_{SS}						
63		$P2_7$					$AN2_7$
64		$P2_6$					$AN2_6$
65		$P2_5$					$AN2_5$
66		$P2_4$					$AN2_4$
67		$P2_3$					$AN2_3$
68		$P2_2$					$AN2_2$
69		$P2_1$					$AN2_1$
70		$P2_0$					$AN2_0$
71		$P1_7$	$\overline{INT5}$				
72		$P1_6$	$\overline{INT4}$				
73		$P1_5$	$\overline{INT3}$				
74		$P1_4$					
75		$P1_3$					
76		$P1_2$					
77		$P1_1$					
78		$P1_0$					
79		$P0_7$					$AN0_7$
80		$P0_6$					$AN0_6$
81		$P0_5$					$AN0_5$
82		$P0_4$					$AN0_4$
83		$P0_3$					$AN0_3$
84		$P0_2$					$AN0_2$
85		$P0_1$					$AN0_1$
86		$P0_0$					$AN0_0$
87		$P10_7$	$\overline{KI_3}$				AN_7
88		$P10_6$	$\overline{KI_2}$				AN_6
89		$P10_5$	$\overline{KI_1}$				AN_5
90		$P10_4$	$\overline{KI_0}$				AN_4
91		$P10_3$					AN_3
92		$P10_2$					AN_2
93		$P10_1$					AN_1
94	AV_{SS}						
95		$P10_0$					AN_0
96	V_{REF}						
97	AV_{CC}						
98		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$
99		$P9_6$			TxD4/SDA4/SRxD4/$CAN1_{OUT}$		ANEX1
100		$P9_5$			CLK4/CAN1IN/$\overline{CAN1WU}$		ANEX0

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Classsfication	Symbol	I/O Type	Function
Power Supply	VCC VSS	I	Apply 4.2 to 5.5 V to both VCC pins. Apply 0 V to the VSS pin
Analog Power Supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS
Reset Input	$\overline{\text{RESET}}$	I	The microcomputer is in a reset state when "L" is applied to the $\overline{\text{RESET}}$ pin
CNVSS	CNVSS	I	Switches processor mode. Connect the CNVSS pin to VSS
Input to Switch External Data Bus Width	BYTE	I	Connect the BYTE pin to VSS
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open.
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To apply external clock, apply it to XCIN and leave XCOUT open
Sub Clock output	XCOUT	O	
Clock Output	CLKOUT	O	Outputs the clock having the same frequency as fC, f8 or f32
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input pins for the $\overline{\text{INT}}$ interrupt
$\overline{\text{NMI}}$ Interrupt Input	$\overline{\text{NMI}}$	I	Input pin for the $\overline{\text{NMI}}$ interrupt
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	Input pins for Timer A0 to A4
Timer B	TB0IN to TB5IN	I	Input pins for Timer B0 to B5
Three-phase Motor Control Timer Output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	Output pins for the three-phase motor control timer
Serial I/O	$\overline{\text{CTS0}}$ to $\overline{\text{CTS4}}$	I	Input pins for data transmission control
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS4}}$	O	Output pins for data reception control
	CLK0 to CLK4	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	Inputs serial data
	TxD0 to TxD4	O	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I^2C Mode	SDA0 to SDA4	I/O	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4		Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)
Serial I/O Special Function	STxD0 to STxD4	O	Outputs serial data when slave mode is selected (STxD2 is a pin for the N-channel open drain output.)
	SRxD0 to SRxD4	I	Inputs serial data when slave mode is selected
	$\overline{\text{SS0}}$ to $\overline{\text{SS4}}$	I	Input pins to control serial I/O special function

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsfication	Symbol	I/O Type	Function
Reference Voltage Input	V_{REF}	I	Applies reference voltage to the A/D converter and D/A converter
A/D Converter	AN_0 to AN_7 $AN0_0$ to $AN0_7$ $AN2_0$ to $AN2_7$	I	Analog input pins for the A/D converter
	$\overline{ADTRG}$	I	Input pin for an external A/D trigger
	ANEX0	I/O	Extended analog input pin for the A/D converter and output pin in external op-amp connection mode
	ANEX1	I	Extended analog input pin for the A/D converter
D/A Converter	DA0, DA1	O	Output pin for the D/A converter
Intelligent I/O	$INPC1_0$ to $INPC1_7$	I	Input pins for the time measurement function
	$OUTC1_0$ to $OUTC1_7$	O	Output pins for the waveform generating function ($OUTC1_6$ and $OUTC1_7$ assigned to $P7_0$ and $P7_1$ are pins for the N-channel open drain output.)
	ISCLK0	I/O	Inputs and outputs the clock for the intelligent I/O communication function
	ISCLK1		
	ISRXD0	I	Inputs data for the intelligent I/O communication function
	ISRXD1		
	ISTXD0	O	Outputs data for the intelligent I/O communication function
	ISTXD1		
	$BE1_{IN}$	I	Inputs data for the intelligent I/O communication function
	$BE1_{OUT}$	O	Outputs data for the intelligent I/O communication function
CAN	$CAN0_{IN}$	I	Input pin for the CAN communication function
	$CAN02_{IN}$		
	$CAN1_{IN}$		
	$CAN2_{IN}$		
	$CAN0_{OUT}$	O	Output pin for the CAN communication function
	$CAN02_{OUT}$		
	$CAN1_{OUT}$		
	$CAN2_{OUT}$		
	$\overline{CAN1WU}$	I	Input pin for the CANi wake-up interrupt (i=1, 2)
	$\overline{CAN2WU}$		
I/O Ports	$P0_0$ to $P0_7$ $P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$ $P4_0$ to $P4_7$ $P5_0$ to $P5_7$	I/O	8-bit I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	$P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P9_0$ to $P9_7$ $P10_0$ to $P10_7$	I/O	I/O ports having equivalent functions to P0 ($P7_0$ and $P7_1$ are ports for the N-channel open drain output.)
	$P8_0$ to $P8_4$ $P8_6$, $P8_7$	I/O	I/O ports having equivalent functions to P0
Input Port	$P8_5$	I	Shares a pin with $\overline{NMI}$. $\overline{NMI}$ input state can be got by reading $P8_5$

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (144-Pin Package Only) (Continued)

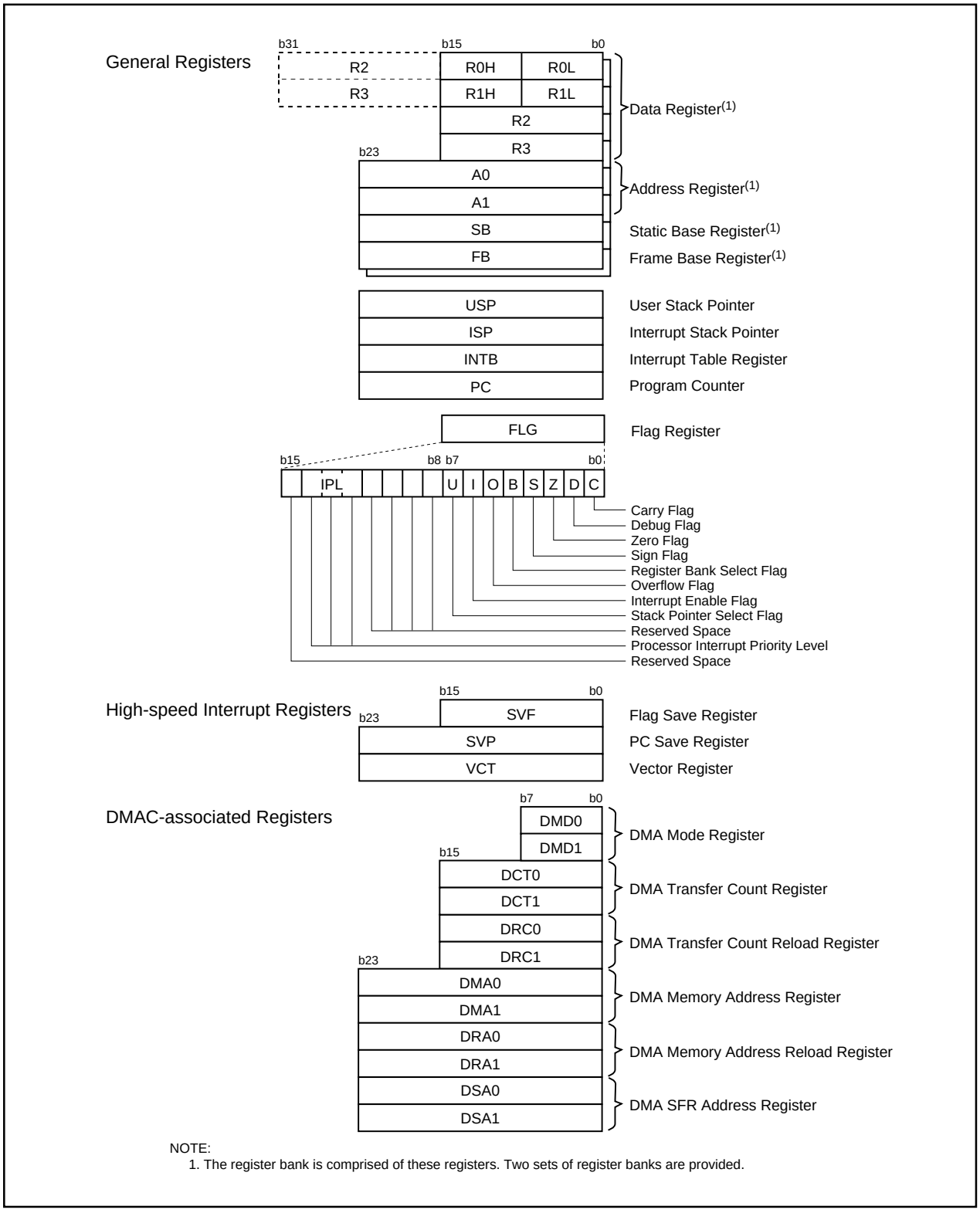
Classsfication	Symbol	I/O Type	Function
A/D Converter	$AN15_0$ to $AN15_7$	I	Analog input pins for the A/D converter
I/O Ports	$P11_0$ to $P11_4$ $P12_0$ to $P12_7$ $P13_0$ to $P13_7$ $P14_0$ to $P14_6$ $P15_0$ to $P15_7$	I/O	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

The register bank is comprised of 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.



NOTE:
1. The register bank is comprised of these registers. Two sets of register banks are provided.

Figure 2.1 CPU Register

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an relocatable interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to **2.1.8 Flag Register (FLG)** for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic operation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic operation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
Interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".
The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When reading, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows:

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows:

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/88 Group (M32C/88T).

The M32C/88 Group (M32C/88T) provides 16-Mbyte address space addressed from 000000$_{16}$ to FFFFFF$_{16}$.

The internal ROM is allocated from address FFFFFF$_{16}$ to lower. For example, a 64-Kbyte internal ROM is addressed from FF0000$_{16}$ to FFFFFF$_{16}$.

The fixed interrupt vectors are allocated from address FFFFDC$_{16}$ to FFFFFF$_{16}$. It stores the starting address of each interrupt routine.

The internal RAM is allocated from address 000400$_{16}$ to higher. For example, a 10-Kbyte internal RAM is allocated from address 000400$_{16}$ to 002BFF$_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFRs, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, timers, is allocated from address 000000$_{16}$ to 0003FF$_{16}$. All blank spaces within SFRs are reserved and cannot be accessed by users.

The special page vectors are addressed from FFFE00$_{16}$ to FFFFDB$_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M32C/80 Series Software Manual** for details.

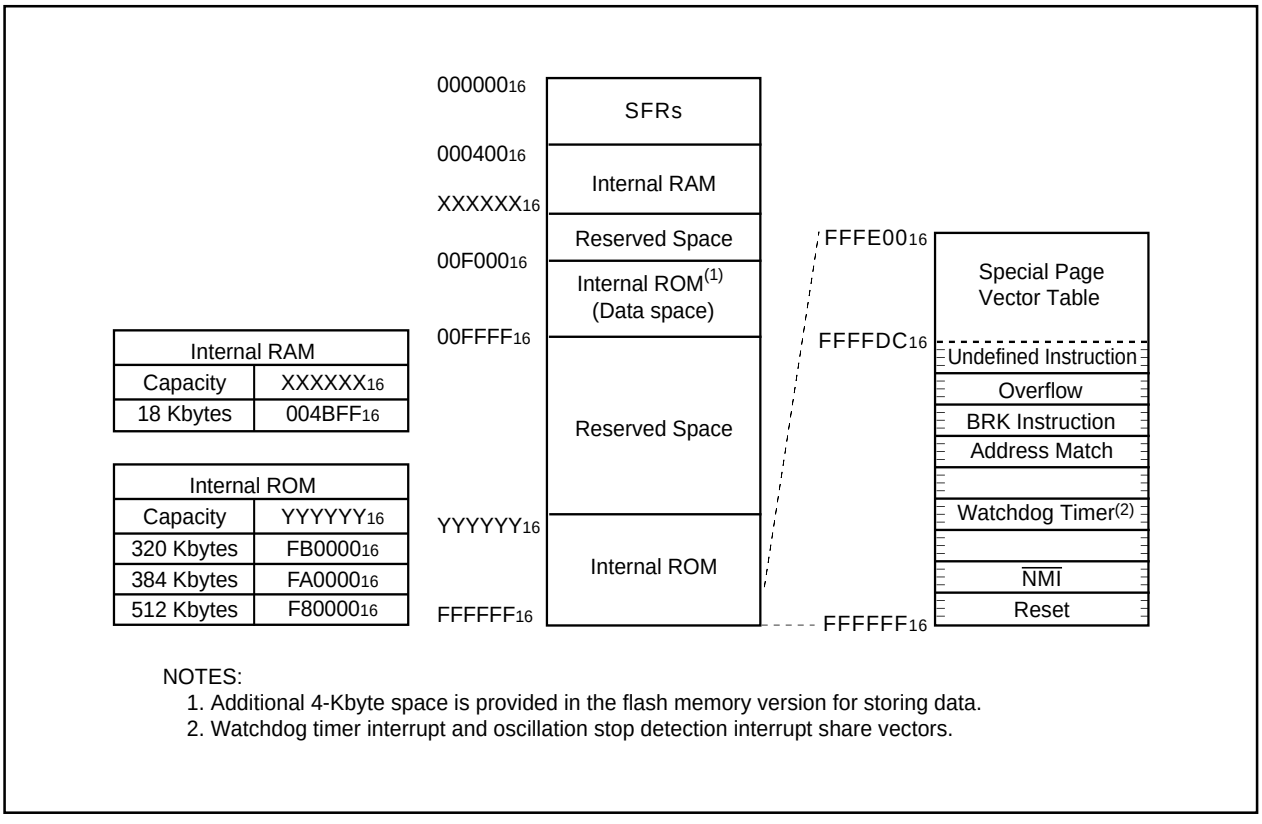


Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

Address	Register	Symbol	Value after RESET
000016			
000116			
000216			
000316			
000416	Processor Mode Register(1)	PM0	1000 00002(CNVss pin ="L")
000516	Processor Mode Register 1	PM1	0016
000616	System Clock Control Register 0	CM0	0000 10002
000716	System Clock Control Register 1	CM1	0010 00002
000816			
000916	Address Match Interrupt Enable Register	AIER	0016
000A16	Protect Register	PRCR	XXXX 00002
000B16			
000C16	Main Clock Division Register	MCD	XXX0 10002
000D16	Oscillation Stop Detection Register	CM2	0016
000E16	Watchdog Timer Start Register	WDTS	XX16
000F16	Watchdog Timer Control Register	WDC	000X XXXX2
001016 001116 001216	Address Match Interrupt Register 0	RMAD0	00000016
001316	Processor Mode Register 2	PM2	0016
001416 001516 001616	Address Match Interrupt Register 1	RMAD1	00000016
001716			
001816 001916 001A16	Address Match Interrupt Register 2	RMAD2	00000016
001B16			
001C16 001D16 001E16	Address Match Interrupt Register 3	RMAD3	00000016
001F16			
002016			
002116			
002216			
002316			
002416			
002516			
002616	PLL Control Register 0	PLC0	0001 X0102
002716	PLL Control Register 1	PLC1	000X 00002
002816 002916 002A16	Address Match Interrupt Register 4	RMAD4	00000016
002B16			
002C16 002D16 002E16	Address Match Interrupt Register 5	RMAD5	00000016
002F16			

X: Indeterminate
Blank spaces are reserved. No access is allowed.
NOTE:
1. The PM01 and PM00 bits in the PM0 register maintain values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
006016			
003016			
003116			
003216			
003316			
003416			
003516			
003616			
003716			
003816 003916 003A16	Address Match Interrupt Register 6	RMAD6	00000016
003B16			
003C16 003D16 003E16	Address Match Interrupt Register 7	RMAD7	00000016
003F16			
004016			
004116			
004216			
004316			
004416			
004516			
004616			
004716			
004816			
004916			
004A16			
004B16			
004C16			
004D16			
004E16			
004F16			
005016			
005116			
005216			
005316			
005416			
005516	Flash Memory Control Register 1	FMR1	0000 01012
005616			
005716	Flash Memory Control Register 0	FMR0	0000 00012
005816			
005916			
005A16			
005B16			
005C16			
005D16			
005E16			
005F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
006016			
006116			
006216			
006316			
006416			
006516			
006616			
006716			
006816	DMA0 Interrupt Control Register	DM0IC	XXXX X0002
006916	Timer B5 Interrupt Control Register	TB5IC	XXXX X0002
006A16	DMA2 Interrupt Control Register	DM2IC	XXXX X0002
006B16	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X0002
006C16	Timer A0 Interrupt Control Register	TA0IC	XXXX X0002
006D16	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X0002
006E16	Timer A2 Interrupt Control Register	TA2IC	XXXX X0002
006F16	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X0002
007016	Timer A4 Interrupt Control Register	TA4IC	XXXX X0002
007116	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X0002
007216	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X0002
007316	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X0002
007416	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X0002
007516	Intelligent I/O Interrupt Control Register 0/ CAN Interrupt 3 Control Register	IIO0IC/ CAN3IC	XXXX X0002
007616	Timer B1 Interrupt Control Register	TB1IC	XXXX X0002
007716	Intelligent I/O Interrupt Control Register 2/ CAN Interrupt 6 Control Register	IIO2IC/ CAN6IC	XXXX X0002
007816	Timer B3 Interrupt Control Register	TB3IC	XXXX X0002
007916	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X0002
007A16	INT5 Interrupt Control Register	INT5IC	XX00 X0002
007B16	CAN Interrupt 8 Control Register	CAN8IC	XXXX X0002
007C16	INT3 Interrupt Control Register	INT3IC	XX00 X0002
007D16	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X0002
007E16	INT1 Interrupt Control Register	INT1IC	XX00 X0002
007F16	Intelligent I/O Interrupt Control Register 10/ CAN Interrupt 1 Control Register	IIO10IC/ CAN1IC	XXXX X0002
008016			
008116	CAN Interrupt 2 Control Register	CAN2IC	XXXX X0002
008216			
008316			
008416			
008516			
008616			
008716			
008816	DMA1 Interrupt Control Register	DM1IC	XXXX X0002
008916	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X0002
008A16	DMA3 Interrupt Control Register	DM3IC	XXXX X0002
008B16	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X0002
008C16	Timer A1 Interrupt Control Register	TA1IC	XXXX X0002
008D16	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X0002
008E16	Timer A3 Interrupt Control Register	TA3IC	XXXX X0002
008F16	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X0002

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
009016	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X0002
009116	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X0002
009216	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X0002
009316	Key Input Interrupt Control Register	KUPIC	XXXX X0002
009416	Timer B0 Interrupt Control Register	TB0IC	XXXX X0002
009516	Intelligent I/O Interrupt Control Register 1/ CAN Interrupt 4 Control Register	IIO1IC/ CAN4IC	XXXX X0002
009616	Timer B2 Interrupt Control Register	TB2IC	XXXX X0002
009716	Intelligent I/O Interrupt Control Register 3/ CAN Interrupt 7 Control Register	IIO3IC/ CAN7IC	XXXX X0002
009816	Timer B4 Interrupt Control Register	TB4IC	XXXX X0002
009916	CAN Interrupt 5 Control Register	CAN5IC	XXXX X0002
009A16	INT4 Interrupt Control Register	INT4IC	XX00 X0002
009B16			
009C16	INT2 Interrupt Control Register	INT2IC	XX00 X0002
009D16	Intelligent I/O Interrupt Control Register 9/ CAN Interrupt 0 Control Register	IIO9IC/ CAN0IC	XXXX X0002
009E16	INT0 Interrupt Control Register	INT0IC	XX00 X0002
009F16	Exit Priority Control Register	RLVL	XXXX 00002
00A016	Interrupt Request Register 0	IIO0IR	0000 000X2
00A116	Interrupt Request Register 1	IIO1IR	0000 000X2
00A216	Interrupt Request Register 2	IIO2IR	0000 000X2
00A316	Interrupt Request Register 3	IIO3IR	0000 000X2
00A416	Interrupt Request Register 4	IIO4IR	0000 000X2
00A516	Interrupt Request Register 5	IIO5IR	0000 000X2
00A616	Interrupt Request Register 6	IIO6IR	0000 000X2
00A716			
00A816	Interrupt Request Register 8	IIO8IR	0000 000X2
00A916	Interrupt Request Register 9	IIO9IR	0000 000X2
00AA16	Interrupt Request Register 10	IIO10IR	0000 000X2
00AB16	Interrupt Request Register 11	IIO11IR	0000 000X2
00AC16			
00AD16			
00AE16			
00AF16			
00B016	Interrupt Enable Register 0	IIO0IE	0016
00B116	Interrupt Enable Register 1	IIO1IE	0016
00B216	Interrupt Enable Register 2	IIO2IE	0016
00B316	Interrupt Enable Register 3	IIO3IE	0016
00B416	Interrupt Enable Register 4	IIO4IE	0016
00B516	Interrupt Enable Register 5	IIO5IE	0016
00B616	Interrupt Enable Register 6	IIO6IE	0016
00B716			
00B816	Interrupt Enable Register 8	IIO8IE	0016
00B916	Interrupt Enable Register 9	IIO9IE	0016
00BA16	Interrupt Enable Register 10	IIO10IE	0016
00BB16	Interrupt Enable Register 11	IIO11IE	0016
00BC16			
00BD16			
00BE16			
00BF16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0₁₆			
00C1₁₆			
00C2₁₆			
00C3₁₆			
00C4₁₆			
00C5₁₆			
00C6₁₆			
00C7₁₆			
00C8₁₆			
00C9₁₆			
00CA₁₆			
00CB₁₆			
00CC₁₆			
00CD₁₆			
00CE₁₆			
00CF₁₆			
00D0₁₆			
00D1₁₆			
00D2₁₆			
00D3₁₆			
00D4₁₆			
00D5₁₆			
00D6₁₆			
00D7₁₆			
00D8₁₆			
00D9₁₆			
00DA₁₆			
00DB₁₆			
00DC₁₆			
00DD₁₆			
00DE₁₆			
00DF₁₆			
00E0₁₆			
00E1₁₆			
00E2₁₆			
00E3₁₆			
00E4₁₆			
00E5₁₆			
00E6₁₆			
00E7₁₆			
00E8₁₆ 00E9₁₆	SI/O Receive Buffer Register 0	G0RB	XXXX XXXX₂ XXX0 XXXX₂
00EA₁₆	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX₁₆
00EB₁₆			
00EC₁₆	Receive Input Register 0	G0RI	XX₁₆
00ED₁₆	SI/O Communication Mode Register 0	G0MR	00₁₆
00EE₁₆	Transmit Output Register 0	G0TO	XX₁₆
00EF₁₆	SI/O Communication Control Register 0	G0CR	0000 X011₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00F016	Data Compare Register 00	G0CMP0	XX16
00F116	Data Compare Register 01	G0CMP1	XX16
00F216	Data Compare Register 02	G0CMP2	XX16
00F316	Data Compare Register 03	G0CMP3	XX16
00F416	Data Mask Register 00	G0MSK0	XX16
00F516	Data Mask Register 01	G0MSK1	XX16
00F616	Communication Clock Select Register	CCS	XXXX 00002
00F716			
00F816	Receive CRC Code Register 0	G0RCRC	XX16
00F916			XX16
00FA16	Transmit CRC Code Register 0	G0TCRC	0016
00FB16			0016
00FC16	SI/O Extended Mode Register 0	G0EMR	0016
00FD16	SI/O Extended Receive Control Register 0	G0ERC	0016
00FE16	SI/O Special Communication Interrupt Detect Register 0	G0IRF	0016
00FF16	SI/O Extended Transmit Control Register 0	G0ETC	0000 0XXX2
010016	Time Measurement/Waveform Generating Register 10	G1TM0/G1PO0	XX16
010116			XX16
010216	Time Measurement/Waveform Generating Register 11	G1TM1/G1PO1	XX16
010316			XX16
010416	Time Measurement/Waveform Generating Register 12	G1TM2/G1PO2	XX16
010516			XX16
010616	Time Measurement/Waveform Generating Register 13	G1TM3/G1PO3	XX16
010716			XX16
010816	Time Measurement/Waveform Generating Register 14	G1TM4/G1PO4	XX16
010916			XX16
010A16	Time Measurement/Waveform Generating Register 15	G1TM5/G1PO5	XX16
010B16			XX16
010C16	Time Measurement/Waveform Generating Register 16	G1TM6/G1PO6	XX16
010D16			XX16
010E16	Time Measurement/Waveform Generating Register 17	G1TM7/G1PO7	XX16
010F16			XX16
011016	Waveform Generating Control Register 10	G1POCR0	0000 X0002
011116	Waveform Generating Control Register 11	G1POCR1	0X00 X0002
011216	Waveform Generating Control Register 12	G1POCR2	0X00 X0002
011316	Waveform Generating Control Register 13	G1POCR3	0X00 X0002
011416	Waveform Generating Control Register 14	G1POCR4	0X00 X0002
011516	Waveform Generating Control Register 15	G1POCR5	0X00 X0002
011616	Waveform Generating Control Register 16	G1POCR6	0X00 X0002
011716	Waveform Generating Control Register 17	G1POCR7	0X00 X0002
011816	Time Measurement Control Register 10	G1TMCR0	0016
011916	Time Measurement Control Register 11	G1TMCR1	0016
011A16	Time Measurement Control Register 12	G1TMCR2	0016
011B16	Time Measurement Control Register 13	G1TMCR3	0016
011C16	Time Measurement Control Register 14	G1TMCR4	0016
011D16	Time Measurement Control Register 15	G1TMCR5	0016
011E16	Time Measurement Control Register 16	G1TMCR6	0016
011F16	Time Measurement Control Register 17	G1TMCR7	0016

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
012016 012116	Base Timer Register 1	G1BT	XX16 XX16
012216	Base Timer Control Register 10	G1BCR0	0016
012316	Base Timer Control Register 11	G1BCR1	X000 000X2
012416	Time Measurement Prescaler Register 16	G1TPR6	0016
012516	Time Measurement Prescaler Register 17	G1TPR7	0016
012616	Function Enable Register 1	G1FE	0016
012716	Function Select Register 1	G1FS	0016
012816 012916	SI/O Receive Buffer Register 1	G1RB	XXXX XXXX2 X000 XXXX2
012A16	Transmit Buffer/Receive Data Register 1	G1TB/G1DR	XX16
012B16			
012C16	Receive Input Register 1	G1RI	XX16
012D16	SI/O Communication Mode Register 1	G1MR	0016
012E16	Transmit Output Register 1	G1TO	XX16
012F16	SI/O Communication Control Register 1	G1CR	0000 X0112
013016	Data Compare Register 10	G1CMP0	XX16
013116	Data Compare Register 11	G1CMP1	XX16
013216	Data Compare Register 12	G1CMP2	XX16
013316	Data Compare Register 13	G1CMP3	XX16
013416	Data Mask Register 10	G1MSK0	XX16
013516	Data Mask Register 11	G1MSK1	XX16
013616			
013716			
013816 013916	Receive CRC Code Register 1	G1RCRC	XX16 XX16
013A16 013B16	Transmit CRC Code Register 1	G1TCRC	0016 0016
013C16	SI/O Extended Mode Register 1	G1EMR	0016
013D16	SI/O Extended Receive Control Register 1	G1ERC	0016
013E16	SI/O Special Communication Interrupt Detection Register 1	G1IRF	0016
013F16	SI/O Extended Transmit Control Register 1	G1ETC	0000 0XXX2
014016			
014116			
014216			
014316			
014416			
014516			
014616			
014716			
014816			
014916			
014A16			
014B16			
014C16			
014D16 to 016F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
017016	CAN2 Slot Buffer Select Register	C2SBS	0016(1)
017116	CAN2 Control Register 1	C2CTLR1	X000 00XX2(1)
017216	CAN2 Sleep Control Register	C2SLPR	XXXX XXX02
017316			
017416 017516	CAN2 Acceptance Filter Support Register	C2AFS	0016(1) 0116(1)
017616			
017716			
017816	Input Function Select Register	IPS	0016
017916	Input Function Select Register A	IPSA	0016
017A16			
017B16			
017C16			
017D16			
017E16			
017F16			
018016	CAN2 Message Slot Buffer 0 Standard ID0	C2SLOT0_0	XX16
018116	CAN2 Message Slot Buffer 0 Standard ID1	C2SLOT0_1	XX16
018216	CAN2 Message Slot Buffer 0 Extended ID0	C2SLOT0_2	XX16
018316	CAN2 Message Slot Buffer 0 Extended ID1	C2SLOT0_3	XX16
018416	CAN2 Message Slot Buffer 0 Extended ID2	C2SLOT0_4	XX16
018516	CAN2 Message Slot Buffer 0 Data Length Code	C2SLOT0_5	XX16
018616	CAN2 Message Slot Buffer 0 Data 0	C2SLOT0_6	XX16
018716	CAN2 Message Slot Buffer 0 Data 1	C2SLOT0_7	XX16
018816	CAN2 Message Slot Buffer 0 Data 2	C2SLOT0_8	XX16
018916	CAN2 Message Slot Buffer 0 Data 3	C2SLOT0_9	XX16
018A16	CAN2 Message Slot Buffer 0 Data 4	C2SLOT0_10	XX16
018B16	CAN2 Message Slot Buffer 0 Data 5	C2SLOT0_11	XX16
018C16	CAN2 Message Slot Buffer 0 Data 6	C2SLOT0_12	XX16
018D16	CAN2 Message Slot Buffer 0 Data 7	C2SLOT0_13	XX16
018E16	CAN2 Message Slot Buffer 0 Time Stamp High-Order	C2SLOT0_14	XX16
018F16	CAN2 Message Slot Buffer 0 Time Stamp Low-Order	C2SLOT0_15	XX16
019016	CAN2 Message Slot Buffer 1 Standard ID0	C2SLOT1_0	XX16
019116	CAN2 Message Slot Buffer 1 Standard ID1	C2SLOT1_1	XX16
019216	CAN2 Message Slot Buffer 1 Extended ID0	C2SLOT1_2	XX16
019316	CAN2 Message Slot Buffer 1 Extended ID1	C2SLOT1_3	XX16
019416	CAN2 Message Slot Buffer 1 Extended ID2	C2SLOT1_4	XX16
019516	CAN2 Message Slot Buffer 1 Data Length Code	C2SLOT1_5	XX16
019616	CAN2 Message Slot Buffer 1 Data 0	C2SLOT1_6	XX16
019716	CAN2 Message Slot Buffer 1 Data 1	C2SLOT1_7	XX16
019816	CAN2 Message Slot Buffer 1 Data 2	C2SLOT1_8	XX16
019916	CAN2 Message Slot Buffer 1 Data 3	C2SLOT1_9	XX16
019A16	CAN2 Message Slot Buffer 1 Data 4	C2SLOT1_10	XX16
019B16	CAN2 Message Slot Buffer 1 Data 5	C2SLOT1_11	XX16
019C16	CAN2 Message Slot Buffer 1 Data 6	C2SLOT1_12	XX16
019D16	CAN2 Message Slot Buffer 1 Data 7	C2SLOT1_13	XX16
019E16	CAN2 Message Slot Buffer 1 Time Stamp High-Order	C2SLOT1_14	XX16
019F16	CAN2 Message Slot Buffer 1 Time Stamp Low-Order	C2SLOT1_15	XX16

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTE:

1. Values are obtained by setting the SLEEP bit in the C2SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
01A0$_{16}$ 01A1$_{16}$	CAN2 Control Register 0	C2CTLR0	XX01 0X01$_2$(2) XXXX 0000$_2$(2)
01A2$_{16}$ 01A3$_{16}$	CAN2 Status Register	C2STR	0000 0000$_2$(2) X000 0X01$_2$(2)
01A4$_{16}$ 01A5$_{16}$	CAN2 Extended ID Register	C2IDR	00$_{16}$(2) 00$_{16}$(2)
01A6$_{16}$ 01A7$_{16}$	CAN2 Configuration Register	C2CONR	0000 XXXX$_2$(2) 0000 0000$_2$(2)
01A8$_{16}$ 01A9$_{16}$	CAN2 Time Stamp Register	C2TSR	00$_{16}$(2) 00$_{16}$(2)
01AA$_{16}$	CAN2 Transmit Error Count Register	C2TEC	00$_{16}$(2)
01AB$_{16}$	CAN2 Receive Error Count Register	C2REC	00$_{16}$(2)
01AC$_{16}$ 01AD$_{16}$	CAN2 Slot Interrupt Status Register	C2SISTR	00$_{16}$(2) 00$_{16}$(2)
01AE$_{16}$			
01AF$_{16}$			
01B0$_{16}$ 01B1$_{16}$	CAN2 Slot Interrupt Mask Register	C2SIMKR	00$_{16}$(2) 00$_{16}$(2)
01B2$_{16}$			
01B3$_{16}$			
01B4$_{16}$	CAN2 Error Interrupt Mask Register	C2EIMKR	XXXX X000$_2$(2)
01B5$_{16}$	CAN2 Error Interrupt Status Register	C2EISTR	XXXX X000$_2$(2)
01B6$_{16}$	CAN2 Error Cause Register	C2EFR	00$_{16}$(2)
01B7$_{16}$	CAN2 Baud Rate Prescaler	C2BRP	0000 0001$_2$(2)
01B8$_{16}$			
01B9$_{16}$	CAN2 Mode Register	C2MDR	XXXX XX00$_2$(2)
01BA$_{16}$			
01BB$_{16}$			
01BC$_{16}$			
01BD$_{16}$			
01BE$_{16}$			
01BF$_{16}$			
01C0$_{16}$ 01C1$_{16}$	CAN2 Single Shot Control Register	C2SSCTLR	00$_{16}$(2) 00$_{16}$(2)
01C2$_{16}$			
01C3$_{16}$			
01C4$_{16}$ 01C5$_{16}$	CAN2 Single Shot Status Register	C2SSSTR	00$_{16}$(2) 00$_{16}$(2)
01C6$_{16}$			
01C7$_{16}$			
01C8$_{16}$	CAN2 Global Mask Register Standard ID0	C2GMR0	XXX0 0000$_2$(2)
01C9$_{16}$	CAN2 Global Mask Register Standard ID1	C2GMR1	XX00 0000$_2$(2)
01CA$_{16}$	CAN2 Global Mask Register Extended ID0	C2GMR2	XXXX 0000$_2$(2)
01CB$_{16}$	CAN2 Global Mask Register Extended ID1	C2GMR3	00$_{16}$(2)
01CC$_{16}$	CAN2 Global Mask Register Extended ID2	C2GMR4	XX00 0000$_2$(2)
01CD$_{16}$			
01CE$_{16}$			
01CF$_{16}$			

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C2CTLR1 register switches functions for addresses 01C0$_{16}$ to 01DF$_{16}$.
2. Values are obtained by setting the SLEEP bit in the C2SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
01D0₁₆	CAN2 Message Slot 0 Control Register / CAN2 Local Mask Register A Standard ID0	C2MCTL0/ C2LMAR0	0000 0000₂(2) XXX0 0000₂(2)
01D1₁₆	CAN2 Message Slot 1 Control Register / CAN2 Local Mask Register A Standard ID1	C2MCTL1/ C2LMAR1	0000 0000₂(2) XX00 0000₂(2)
01D2₁₆	CAN2 Message Slot 2 Control Register / CAN2 Local Mask Register A Extended ID0	C2MCTL2/ C2LMAR2	0000 0000₂(2) XXXX 0000₂(2)
01D3₁₆	CAN2 Message Slot 3 Control Register / CAN2 local Mask Register A Extended ID1	C2MCTL3/ C2LMAR3	00₁₆(2) 00₁₆(2)
01D4₁₆	CAN2 Message Slot 4 Control Register / CAN2 Local Mask Register A Extended ID2	C2MCTL4/ C2LMAR4	0000 0000₂(2) XX00 0000₂(2)
01D5₁₆	CAN2 Message Slot 5 Control Register	C2MCTL5	00₁₆(2)
01D6₁₆	CAN2 Message Slot 6 Control Register	C2MCTL6	00₁₆(2)
01D7₁₆	CAN2 Message Slot 7 Control Register	C2MCTL7	00₁₆(2)
01D8₁₆	CAN2 Message Slot 8 Control Register / CAN2 Local Mask Register B Standard ID0	C2MCTL8/ C2LMBR0	0000 0000₂(2) XXX0 0000₂(2)
01D9₁₆	CAN2 Message Slot 9 Control Register / CAN2 Local Mask Register B Standard ID1	C2MCTL9/ C2LMBR1	0000 0000₂(2) XX00 0000₂(2)
01DA₁₆	CAN2 Message Slot 10 Control Register / CAN2 Local Mask Register B Extended ID2	C2MCTL10/ C2LMBR2	0000 0000₂(2) XXXX 0000₂(2)
01DB₁₆	CAN2 Message Slot 11 Control Register / CAN2 Local Mask Register B Extended ID3	C2MCTL11/ C2LMBR3	00₁₆(2) 00₁₆(2)
01DC₁₆	CAN2 Message Slot 12 Control Register / CAN2 Local Mask Register B Extended ID4	C2MCTL12/ C2LMBR4	0000 0000₂(2) XX00 0000₂(2)
01DD₁₆	CAN2 Message Slot 13 Control Register	C2MCTL13	00₁₆(2)
01DE₁₆	CAN2 Message Slot 14 Control Register	C2MCTL14	00₁₆(2)
01DF₁₆	CAN2 Message Slot 15 Control Register	C2MCTL15	00₁₆(2)

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C2CTLR1 register switches functions for addresses 01C0₁₆ to 01DF₁₆.
2. Values are obtained by setting the SLEEP bit in the C2SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
01E0₁₆	CAN0 Message Slot Buffer 0 Standard ID0	C0SLOT0_0	XX₁₆
01E1₁₆	CAN0 Message Slot Buffer 0 Standard ID1	C0SLOT0_1	XX₁₆
01E2₁₆	CAN0 Message Slot Buffer 0 Extended ID0	C0SLOT0_2	XX₁₆
01E3₁₆	CAN0 Message Slot Buffer 0 Extended ID1	C0SLOT0_3	XX₁₆
01E4₁₆	CAN0 Message Slot Buffer 0 Extended ID2	C0SLOT0_4	XX₁₆
01E5₁₆	CAN0 Message Slot Buffer 0 Data Length Code	C0SLOT0_5	XX₁₆
01E6₁₆	CAN0 Message Slot Buffer 0 Data 0	C0SLOT0_6	XX₁₆
01E7₁₆	CAN0 Message Slot Buffer 0 Data 1	C0SLOT0_7	XX₁₆
01E8₁₆	CAN0 Message Slot Buffer 0 Data 2	C0SLOT0_8	XX₁₆
01E9₁₆	CAN0 Message Slot Buffer 0 Data 3	C0SLOT0_9	XX₁₆
01EA₁₆	CAN0 Message Slot Buffer 0 Data 4	C0SLOT0_10	XX₁₆
01EB₁₆	CAN0 Message Slot Buffer 0 Data 5	C0SLOT0_11	XX₁₆
01EC₁₆	CAN0 Message Slot Buffer 0 Data 6	C0SLOT0_12	XX₁₆
01ED₁₆	CAN0 Message Slot Buffer 0 Data 7	C0SLOT0_13	XX₁₆
01EE₁₆	CAN0 Message Slot Buffer 0 Time Stamp High-Order	C0SLOT0_14	XX₁₆
01EF₁₆	CAN0 Message Slot Buffer 0 Time Stamp Low-Order	C0SLOT0_15	XX₁₆
01F0₁₆	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XX₁₆
01F1₁₆	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XX₁₆
01F2₁₆	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XX₁₆
01F3₁₆	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XX₁₆
01F4₁₆	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XX₁₆
01F5₁₆	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XX₁₆
01F6₁₆	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XX₁₆
01F7₁₆	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XX₁₆
01F8₁₆	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XX₁₆
01F9₁₆	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XX₁₆
01FA₁₆	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XX₁₆
01FB₁₆	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XX₁₆
01FC₁₆	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XX₁₆
01FD₁₆	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XX₁₆
01FE₁₆	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XX₁₆
01FF₁₆	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XX₁₆
0200₁₆ 0201₁₆	CAN0 Control Register 0	C0CTLR0	XX01 0X01₂(1) XXXX 0000₂(1)
0202₁₆ 0203₁₆	CAN0 Status Register	C0STR	0000 0000₂(1) X000 0X01₂(1)
0204₁₆ 0205₁₆	CAN0 Extended ID Register	C0IDR	00₁₆(1) 00₁₆(1)
0206₁₆ 0207₁₆	CAN0 Configuration Register	C0CONR	0000 XXXX₂(1) 0000 0000₂(1)
0208₁₆ 0209₁₆	CAN0 Time Stamp Register	C0TSR	00₁₆(1) 00₁₆(1)
020A₁₆	CAN0 Transmit Error Count Register	C0TEC	00₁₆(1)
020B₁₆	CAN0 Receive Error Count Register	C0REC	00₁₆(1)
020C₁₆ 020D₁₆	CAN0 Slot Interrupt Status Register	C0SISTR	00₁₆(1) 00₁₆(1)
020E₁₆			
020F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTE:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
021016 021116	CAN0 Slot Interrupt Mask Register	C0SIMKR	0016(2) 0016(2)
021216			
021316			
021416	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X0002(2)
021516	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X0002(2)
021616	CAN0 Error Cause Register	C0EFR	0016(2)
021716	CAN0 Baud Rate Prescaler	C0BRP	0000 00012(2)
021816			
021916	CAN0 Mode Register	C0MDR	XXXX XX002(2)
021A16			
021B16			
021C16			
021D16			
021E16			
021F16			
022016 022116	CAN0 Single Shot Control Register	C0SSCTLR	0016(2) 0016(2)
022216			
022316			
022416 022516	CAN0 Single Shot Status Register	C0SSSTR	0016(2) 0016(2)
022616			
022716			
022816	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 00002(2)
022916	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 00002(2)
022A16	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 00002(2)
022B16	CAN0 Global Mask Register Extended ID1	C0GMR3	0016(2)
022C16	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 00002(2)
022D16			
022E16			
022F16			
023016	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 00002(2) XXX0 00002(2)
023116	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 00002(2) XX00 00002(2)
023216	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 00002(2) XXXX 00002(2)
023316	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	0016(2) 0016(2)
023416	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 00002(2) XX00 00002(2)
023516	CAN0 Message Slot 5 Control Register	C0MCTL5	0016(2)
023616	CAN0 Message Slot 6 Control Register	C0MCTL6	0016(2)
023716	CAN0 Message Slot 7 Control Register	C0MCTL7	0016(2)
023816	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 00002(2) XXX0 00002(2)
023916	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 00002(2) XX00 00002(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
023A16	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10/ C0LMBR2	0000 00002(2) XXXX 00002(2)
023B16	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11/ C0LMBR3	0016(2) 0016(2)
023C16	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12/ C0LMBR4	0000 00002(2) XX00 00002(2)
023D16	CAN0 Message Slot 13 Control Register	C0MCTL13	0016(2)
023E16	CAN0 Message Slot 14 Control Register	C0MCTL14	0016(2)
023F16	CAN0 Message Slot 15 Control Register	C0MCTL15	0016(2)
024016	CAN0 Slot Buffer Select Register	C0SBS	0016(2)
024116	CAN0 Control Register 1	C0CTLR1	X000 00XX2(2)
024216	CAN0 Sleep Control Register	C0SLPR	XXXX XXX02
024316			
024416 024516	CAN0 Acceptance Filter Support Register	C0AFS	0016(2) 0116(2)
024616			
024716			
024816			
024916			
024A16			
024B16			
024C16			
024D16			
024E16			
024F16			
025016	CAN1 Slot Buffer Select Register	C1SBS	0016(3)
025116	CAN1 Control Register 1	C1CTLR1	X000 00XX2(3)
025216	CAN1 Sleep Control Register	C1SLPR	XXXX XXX02(3)
025316			
025416 025516	CAN1 Acceptance Filter Support Register	C1AFS	0016(3) 0116(3)
025616			
025716			
025816			
025916			
025A16			
025B16			
025C16			
025D16			
025E16			
025F16			

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.
3. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
026016	CAN1 Message Slot Buffer 0 Standard ID0	C1SLOT0_0	XX16
026116	CAN1 Message Slot Buffer 0 Standard ID1	C1SLOT0_1	XX16
026216	CAN1 Message Slot Buffer 0 Extended ID0	C1SLOT0_2	XX16
026316	CAN1 Message Slot Buffer 0 Extended ID1	C1SLOT0_3	XX16
026416	CAN1 Message Slot Buffer 0 Extended ID2	C1SLOT0_4	XX16
026516	CAN1 Message Slot Buffer 0 Data Length Code	C1SLOT0_5	XX16
026616	CAN1 Message Slot Buffer 0 Data 0	C1SLOT0_6	XX16
026716	CAN1 Message Slot Buffer 0 Data 1	C1SLOT0_7	XX16
026816	CAN1 Message Slot Buffer 0 Data 2	C1SLOT0_8	XX16
026916	CAN1 Message Slot Buffer 0 Data 3	C1SLOT0_9	XX16
026A16	CAN1 Message Slot Buffer 0 Data 4	C1SLOT0_10	XX16
026B16	CAN1 Message Slot Buffer 0 Data 5	C1SLOT0_11	XX16
026C16	CAN1 Message Slot Buffer 0 Data 6	C1SLOT0_12	XX16
026D16	CAN1 Message Slot Buffer 0 Data 7	C1SLOT0_13	XX16
026E16	CAN1 Message Slot Buffer 0 Time Stamp High-Order	C1SLOT0_14	XX16
026F16	CAN1 Message Slot Buffer 0 Time Stamp Low-Order	C1SLOT0_15	XX16
027016	CAN1 Message Slot Buffer 1 Standard ID0	C1SLOT1_0	XX16
027116	CAN1 Message Slot Buffer 1 Standard ID1	C1SLOT1_1	XX16
027216	CAN1 Message Slot Buffer 1 Extended ID0	C1SLOT1_2	XX16
027316	CAN1 Message Slot Buffer 1 Extended ID1	C1SLOT1_3	XX16
027416	CAN1 Message Slot Buffer 1 Extended ID2	C1SLOT1_4	XX16
027516	CAN1 Message Slot Buffer 1 Data Length Code	C1SLOT1_5	XX16
027616	CAN1 Message Slot Buffer 1 Data 0	C1SLOT1_6	XX16
027716	CAN1 Message Slot Buffer 1 Data 1	C1SLOT1_7	XX16
027816	CAN1 Message Slot Buffer 1 Data 2	C1SLOT1_8	XX16
027916	CAN1 Message Slot Buffer 1 Data 3	C1SLOT1_9	XX16
027A16	CAN1 Message Slot Buffer 1 Data 4	C1SLOT1_10	XX16
027B16	CAN1 Message Slot Buffer 1 Data 5	C1SLOT1_11	XX16
027C16	CAN1 Message Slot Buffer 1 Data 6	C1SLOT1_12	XX16
027D16	CAN1 Message Slot Buffer 1 Data 7	C1SLOT1_13	XX16
027E16	CAN1 Message Slot Buffer 1 Time Stamp High-Order	C1SLOT1_14	XX16
027F16	CAN1 Message Slot Buffer 1 Time Stamp Low-Order	C1SLOT1_15	XX16
028016 028116	CAN1 Control Register 0	C1CTLR0	XX01 0X012(1) XXXX 00002(1)
028216 028316	CAN1 Status Register	C1STR	0000 00002(1) X000 0X012(1)
028416 028516	CAN1 Extended ID Register	C1IDR	0016(1) 0016(1)
028616 028716	CAN1 Configuration Register	C1CONR	0000 XXXX2(1) 0000 00002(1)
028816 028916	CAN1 Time Stamp Register	C1TSR	0016(1) 0016(1)
028A16	CAN1 Transmit Error Count Register	C1TEC	0016(1)
028B16	CAN1 Receive Error Count Register	C1REC	0016(1)
028C16 028D16	CAN1 Slot Interrupt Status Register	C1SISTR	0016(1) 0016(1)
028E16			
028F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTE:

1. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
029016 029116	CAN1 Slot Interrupt Mask Register	C1SIMKR	0016(2) 0016(2)
029216			
029316			
029416	CAN1 Error Interrupt Mask Register	C1EIMKR	XXXX X0002(2)
029516	CAN1 Error Interrupt Status Register	C1EISTR	XXXX X0002(2)
029616	CAN1 Error Factor Register	C1EFR	0016(2)
029716	CAN1 Baud Rate Prescaler	C1BRP	0000 00012(2)
029816			
029916	CAN1 Mode Register	C1MDR	XXXX XX002(2)
029A16			
029B16			
029C16			
029D16			
029E16			
029F16			
02A016 02A116	CAN1 Single Shot Control Register	C1SSCTLR	0016(2) 0016(2)
02A216			
02A316			
02A416 02A516	CAN1 Single Shot Status Register	C1SSSTR	0016(2) 0016(2)
02A616			
02A716			
02A816	CAN1 Global Mask Register Standard ID0	C1GMR0	XXX0 00002(2)
02A916	CAN1 Global Mask Register Standard ID1	C1GMR1	XX00 00002(2)
02AA16	CAN1 Global Mask Register Extended ID0	C1GMR2	XXXX 00002(2)
02AB16	CAN1 Global Mask Register Extended ID1	C1GMR3	0016(2)
02AC16	CAN1 Global Mask Register Extended ID2	C1GMR4	XX00 00002(2)
02AD16			
02AE16			
02AF16			
02B016	CAN1 Message Slot 0 Control Register / CAN1 Local Mask Register A Standard ID0	C1MCTL0/ C1LMAR0	0000 00002(2) XXX0 00002(2)
02B116	CAN1 Message Slot 1 Control Register / CAN1 Local Mask Register A Standard ID1	C1MCTL1/ C1LMAR1	0000 00002(2) XX00 00002(2)
02B216	CAN1 Message Slot 2 Control Register / CAN1 Local Mask Register A Extended ID0	C1MCTL2/ C1LMAR2	0000 00002(2) XXXX 00002(2)
02B316	CAN1 Message Slot 3 Control Register / CAN1 Local Mask Register A Extended ID1	C1MCTL3/ C1LMAR3	0016(2) 0016(2)
02B416	CAN1 Message Slot 4 Control Register / CAN1 Local Mask Register A Extended ID2	C1MCTL4/ C1LMAR4	0000 00002(2) XX00 00002(2)
02B516	CAN1 Message Slot 5 Control Register	C1MCTL5	0016(2)
02B616	CAN1 Message Slot 6 Control Register	C1MCTL6	0016(2)
02B716	CAN1 Message Slot 7 Control Register	C1MCTL7	0016(2)
02B816	CAN1 Message Slot 8 Control Register / CAN1 Local Mask Register B Standard ID0	C1MCTL8/ C1LMBR0	0000 00002(2) XXX0 00002(2)
02B916	CAN1 Message Slot 9 Control Register / CAN1 Local Mask Register B Standard ID1	C1MCTL9/ C1LMBR1	0000 00002(2) XX00 00002(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C1CTLR1 register switches functions for addresses 02A016 to 02BF16.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
02BA16	CAN1 Message Slot 10 Control Register / CAN1 Local Mask Register B Extended ID0	C1MCTL10/ C1LMBR2	0000 00002(2) XXXX 00002(2)
02BB16	CAN1 Message Slot 11 Control Register / CAN1 Local Mask Register B Extended ID1	C1MCTL11/ C1LMBR3	0016(2) 0016(2)
02BC16	CAN1 Message Slot 12 Control Register / CAN1 Local Mask Register B Extended ID2	C1MCTL12/ C1LMBR4	0000 00002(2) XX00 00002(2)
02BD16	CAN1 Message Slot 13 Control Register	C1MCTL13	0016(2)
02BE16	CAN1 Message Slot 14 Control Register	C1MCTL14	0016(2)
02BF16	CAN1 Message Slot 15 Control Register	C1MCTL15	0016(2)
02C016 02C116	X0 Register Y0 Register	X0R,Y0R	XX16 XX16
02C216 02C316	X1 Register Y1 Register	X1R,Y1R	XX16 XX16
02C416 02C516	X2 Register Y2 Register	X2R,Y2R	XX16 XX16
02C616 02C716	X3 Register Y3 Register	X3R,Y3R	XX16 XX16
02C816 02C916	X4 Register Y4 Register	X4R,Y4R	XX16 XX16
02CA16 02CB16	X5 Register Y5 Register	X5R,Y5R	XX16 XX16
02CC16 02CD16	X6 Register Y6 Register	X6R,Y6R	XX16 XX16
02CE16 02CF16	X7 Register Y7 Register	X7R,Y7R	XX16 XX16
02D016 02D116	X8 Register Y8 Register	X8R,Y8R	XX16 XX16
02D216 02D316	X9 Register Y9 Register	X9R,Y9R	XX16 XX16
02D416 02D516	X10 Register Y10 Register	X10R,Y10R	XX16 XX16
02D616 02D716	X11 Register Y11 Register	X11R,Y11R	XX16 XX16
02D816 02D916	X12 Register Y12 Register	X12R,Y12R	XX16 XX16
02DA16 02DB16	X13 Register Y13 Register	X13R,Y13R	XX16 XX16
02DC16 02DD16	X14 Register Y14 Register	X14R,Y14R	XX16 XX16
02DE16 02DF16	X15 Register Y15 Register	X15R,Y15R	XX16 XX16

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C1CTLR1 register switches functions for addresses 02A016 to 02BF16.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying a clock to the CAN module.

Address	Register	Symbol	Value after RESET
02E0₁₆	X/Y Control Register	XYC	XXXX XX00₂
02E1₁₆			
02E2₁₆			
02E3₁₆			
02E4₁₆	UART1 Special Mode Register 4	U1SMR4	00₁₆
02E5₁₆	UART1 Special Mode Register 3	U1SMR3	00₁₆
02E6₁₆	UART1 Special Mode Register 2	U1SMR2	00₁₆
02E7₁₆	UART1 Special Mode Register	U1SMR	00₁₆
02E8₁₆	UART1 Transmit/Receive Mode Register	U1MR	00₁₆
02E9₁₆	UART1 Bit Rate Register	U1BRG	XX₁₆
02EA₁₆ 02EB₁₆	UART1 Transmit Buffer Register	U1TB	XX₁₆ XX₁₆
02EC₁₆	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000₂
02ED₁₆	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010₂
02EE₁₆ 02EF₁₆	UART1 Receive Buffer Register	U1RB	XX₁₆ XX₁₆
02F0₁₆			
02F1₁₆			
02F2₁₆			
02F3₁₆			
02F4₁₆	UART4 Special Mode Register 4	U4SMR4	00₁₆
02F5₁₆	UART4 Special Mode Register 3	U4SMR3	00₁₆
02F6₁₆	UART4 Special Mode Register 2	U4SMR2	00₁₆
02F7₁₆	UART4 Special Mode Register	U4SMR	00₁₆
02F8₁₆	UART4 Transmit/Receive Mode Register	U4MR	00₁₆
02F9₁₆	UART4 Bit Rate Register	U4BRG	XX₁₆
02FA₁₆ 02FB₁₆	UART4 Transmit Buffer Register	U4TB	XX₁₆ XX₁₆
02FC₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000₂
02FD₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010₂
02FE₁₆ 02FF₁₆	UART4 Receive Buffer Register	U4RB	XX₁₆ XX₁₆
0300₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX₂
0301₁₆			
0302₁₆ 0303₁₆	Timer A1-1 Register	TA11	XX₁₆ XX₁₆
0304₁₆ 0305₁₆	Timer A2-1 Register	TA21	XX₁₆ XX₁₆
0306₁₆ 0307₁₆	Timer A4-1 Register	TA41	XX₁₆ XX₁₆
0308₁₆	Three-Phase PWM Control Register 0	INVC0	00₁₆
0309₁₆	Three-Phase PWM Control Register 1	INVC1	00₁₆
030A₁₆	Three-Phase Output Buffer Register 0	IDB0	XX11 1111₂
030B₁₆	Three-Phase Output Buffer Register 1	IDB1	XX11 1111₂
030C₁₆	Dead Time Timer	DTT	XX₁₆
030D₁₆	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX₁₆
030E₁₆			
030F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
031016	Timer B3 Register	TB3	XX16
031116			XX16
031216	Timer B4 Register	TB4	XX16
031316			XX16
031416	Timer B5 Register	TB5	XX16
031516			XX16
031616			
031716			
031816			
031916			
031A16			
031B16	Timer B3 Mode Register	TB3MR	00XX 00002
031C16	Timer B4 Mode Register	TB4MR	00XX 00002
031D16	Timer B5 Mode Register	TB5MR	00XX 00002
031E16			
031F16	External Interrupt Request Source Select Register	IFSR	0016
032016			
032116			
032216			
032316			
032416	UART3 Special Mode Register 4	U3SMR4	0016
032516	UART3 Special Mode Register 3	U3SMR3	0016
032616	UART3 Special Mode Register 2	U3SMR2	0016
032716	UART3 Special Mode Register	U3SMR	0016
032816	UART3 Transmit/Receive Mode Register	U3MR	0016
032916	UART3 Bit Rate Register	U3BRG	XX16
032A16	UART3 Transmit Buffer Register	U3TB	XX16
032B16			XX16
032C16	UART3 Transmit/Receive Control Register 0	U3C0	0000 10002
032D16	UART3 Transmit/Receive Control Register 1	U3C1	0000 00102
032E16	UART3 Receive Buffer Register	U3RB	XX16
032F16			XX16
033016			
033116			
033216			
033316			
033416	UART2 Special Mode Register 4	U2SMR4	0016
033516	UART2 Special Mode Register 3	U2SMR3	0016
033616	UART2 Special Mode Register 2	U2SMR2	0016
033716	UART2 Special Mode Register	U2SMR	0016
033816	UART2 Transmit/Receive Mode Register	U2MR	0016
033916	UART2 Bit Rate Register	U2BRG	XX16
033A16	UART2 Transmit Buffer Register	U2TB	XX16
033B16			XX16
033C16	UART2 Transmit/Receive Control Register 0	U2C0	0000 10002
033D16	UART2 Transmit/Receive Control Register 1	U2C1	0000 00102
033E16	UART2 Receive Buffer Register	U2RB	XX16
033F16			XX16

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
034016	Count Start Flag	TABSR	0016
034116	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX2
034216	One-Shot Start Flag	ONSF	0016
034316	Trigger Select Register	TRGSR	0016
034416	Up/Down Flag	UDF	0016
034516			
034616 034716	Timer A0 Register	TA0	XX16 XX16
034816 034916	Timer A1 Register	TA1	XX16 XX16
034A16 034B16	Timer A2 Register	TA2	XX16 XX16
034C16 034D16	Timer A3 Register	TA3	XX16 XX16
034E16 034F16	Timer A4 Register	TA4	XX16 XX16
035016 035116	Timer B0 Register	TB0	XX16 XX16
035216 035316	Timer B1 Register	TB1	XX16 XX16
035416 035516	Timer B2 Register	TB2	XX16 XX16
035616	Timer A0 Mode Register	TA0MR	0016
035716	Timer A1 Mode Register	TA1MR	0016
035816	Timer A2 Mode Register	TA2MR	0016
035916	Timer A3 Mode Register	TA3MR	0016
035A16	Timer A4 Mode Register	TA4MR	0016
035B16	Timer B0 Mode Register	TB0MR	00XX 00002
035C16	Timer B1 Mode Register	TB1MR	00XX 00002
035D16	Timer B2 Mode Register	TB2MR	00XX 00002
035E16	Timer B2 Special Mode Register	TB2SC	XXXX XXX02
035F16	Count Source Prescaler Register(1)	TCSPR	0XXX 00002
036016			
036116			
036216			
036316			
036416	UART0 Special Mode Register 4	U0SMR4	0016
036516	UART0 Special Mode Register 3	U0SMR3	0016
036616	UART0 Special Mode Register 2	U0SMR2	0016
036716	UART0 Special Mode Register	U0SMR	0016
036816	UART0 Transmit/Receive Mode Register	U0MR	0016
036916	UART0 Bit Rate Register	U0BRG	XX16
036A16 036B16	UART0 Transmit Buffer Register	U0TB	XX16 XX16
036C16	UART0 Transmit/Receive Control Register 0	U0C0	0000 10002
036D16	UART0 Transmit/Receive Control Register 1	U0C1	0000 00102
036E16 036F16	UART0 Receive Buffer Register	U0RB	XX16 XX16

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTE:

1. The TCSPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
037016			
037116			
037216			
037316			
037416			
037516			
037616			
037716			
037816	DMA0 Request Source Select Register	DM0SL	0X00 00002
037916	DMA1 Request Source Select Register	DM1SL	0X00 00002
037A16	DMA2 Request Source Select Register	DM2SL	0X00 00002
037B16	DMA3 Request Source Select Register	DM3SL	0X00 00002
037C16 037D16	CRC Data Register	CRCD	XX16 XX16
037E16	CRC Input Register	CRCIN	XX16
037F16			
038016 038116	A/D0 Register 0	AD00	XXXX XXXX2 0000 00002
038216 038316	A/D0 Register 1	AD01	XX16 XX16
038416 038516	A/D0 Register 2	AD02	XX16 XX16
038616 038716	A/D0 Register 3	AD03	XX16 XX16
038816 038916	A/D0 Register 4	AD04	XX16 XX16
038A16 038B16	A/D0 Register 5	AD05	XX16 XX16
038C16 038D16	A/D0 Register 6	AD06	XX16 XX16
038E16 038F16	A/D0 Register 7	AD07	XX16 XX16
039016			
039116			
039216	A/D0 Control Register 4	AD0CON4	XXXX 00XX2
039316			
039416	A/D0 Control Register 2	AD0CON2	XX0X X0002
039516	A/D0 Control Register 3	AD0CON3	XXXX X0002
039616	A/D0 Control Register 0	AD0CON0	0016
039716	A/D0 Control Register 1	AD0CON1	0016
039816	D/A Register 0	DA0	XX16
039916			
039A16	D/A Register 1	DA1	XX16
039B16			
039C16	D/A Control Register	DACON	XXXX XX002
039D16			
039E16			
039F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03A0₁₆	Function Select Register A8	PS8	X000 0000₂
03A1₁₆	Function Select Register A9	PS9	00₁₆
03A2₁₆			
03A3₁₆			
03A4₁₆			
03A5₁₆			
03A6₁₆			
03A7₁₆	Function Select Register D1	PSD1	X0XX XX00₂
03A8₁₆			
03A9₁₆			
03AA₁₆			
03AB₁₆			
03AC₁₆	Function Select Register C2	PSC2	XXXX X00X₂
03AD₁₆	Function Select Register C3	PSC3	X0XX XXXX₂
03AE₁₆			
03AF₁₆	Function Select Register C	PSC	00X0 0000₂
03B0₁₆	Function Select Register A0	PS0	00₁₆
03B1₁₆	Function Select Register A1	PS1	00₁₆
03B2₁₆	Function Select Register B0	PSL0	00₁₆
03B3₁₆	Function Select Register B1	PSL1	00₁₆
03B4₁₆	Function Select Register A2	PS2	00X0 0000₂
03B5₁₆	Function Select Register A3	PS3	00₁₆
03B6₁₆	Function Select Register B2	PSL2	00X0 0000₂
03B7₁₆	Function Select Register B3	PSL3	00₁₆
03B8₁₆			
03B9₁₆	Function Select Register A5	PS5	XXX0 0000₂
03BA₁₆			
03BB₁₆			
03BC₁₆			
03BD₁₆			
03BE₁₆			
03BF₁₆			
03C0₁₆	Port P6 Register	P6	XX₁₆
03C1₁₆	Port P7 Register	P7	XX₁₆
03C2₁₆	Port P6 Direction Register	PD6	00₁₆
03C3₁₆	Port P7 Direction Register	PD7	00₁₆
03C4₁₆	Port P8 Register	P8	XX₁₆
03C5₁₆	Port P9 Register	P9	XX₁₆
03C6₁₆	Port P8 Direction Register	PD8	00X0 0000₂
03C7₁₆	Port P9 Direction Register	PD9	00₁₆
03C8₁₆	Port P10 Register	P10	XX₁₆
03C9₁₆	Port P11 Register	P11	XX₁₆
03CA₁₆	Port P10 Direction Register	PD10	00₁₆
03CB₁₆	Port P11 Direction Register	PD11	XXX0 0000₂
03CC₁₆	Port P12 Register	P12	XX₁₆
03CD₁₆	Port P13 Register	P13	XX₁₆
03CE₁₆	Port P12 Direction Register	PD12	00₁₆
03CF₁₆	Port P13 Direction Register	PD13	00₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03D0₁₆	Port P14 Register	P14	XX₁₆
03D1₁₆	Port P15 Register	P15	XX₁₆
03D2₁₆	Port P14 Direction Register	PD14	X000 0000₂
03D3₁₆	Port P15 Direction Register	PD15	00₁₆
03D4₁₆			
03D5₁₆			
03D6₁₆			
03D7₁₆			
03D8₁₆			
03D9₁₆			
03DA₁₆	Pull-Up Control Register 2	PUR2	00₁₆
03DB₁₆	Pull-Up Control Register 3	PUR3	00₁₆
03DC₁₆	Pull-Up Control Register 4	PUR4	XXXX 0000₂
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 Register	P0	XX₁₆
03E1₁₆	Port P1 Register	P1	XX₁₆
03E2₁₆	Port P0 Direction Register	PD0	00₁₆
03E3₁₆	Port P1 Direction Register	PD1	00₁₆
03E4₁₆	Port P2 Register	P2	XX₁₆
03E5₁₆	Port P3 Register	P3	XX₁₆
03E6₁₆	Port P2 Direction Register	PD2	00₁₆
03E7₁₆	Port P3 Direction Register	PD3	00₁₆
03E8₁₆	Port P4 Register	P4	XX₁₆
03E9₁₆	Port P5 Register	P5	XX₁₆
03EA₁₆	Port P4 Direction Register	PD4	00₁₆
03EB₁₆	Port P5 Direction Register	PD5	00₁₆
03EC₁₆			
03ED₁₆			
03EE₁₆			
03EF₁₆			
03F0₁₆	Pull-Up Control Register 0	PUR0	00₁₆
03F1₁₆	Pull-Up Control Register 1	PUR1	XXXX 0000₂
03F2₁₆			
03F3₁₆			
03F4₁₆			
03F5₁₆			
03F6₁₆			
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆			
03FD₁₆			
03FE₁₆			
03FF₁₆	Port Control Register	PCR	XXXX XXX0₂

X: Indeterminate

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<100-pin package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$			
03A1$_{16}$			
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function Select Register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function Select Register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function Select Register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function Select Register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function Select Register A0	PS0	00$_{16}$
03B1$_{16}$	Function Select Register A1	PS1	00$_{16}$
03B2$_{16}$	Function Select Register B0	PSL0	00$_{16}$
03B3$_{16}$	Function Select Register B1	PSL1	00$_{16}$
03B4$_{16}$	Function Select Register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function Select Register A3	PS3	00$_{16}$
03B6$_{16}$	Function Select Register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function Select Register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$			
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 Register	P6	XX$_{16}$
03C1$_{16}$	Port P7 Register	P7	XX$_{16}$
03C2$_{16}$	Port P6 Direction Register	PD6	00$_{16}$
03C3$_{16}$	Port P7 Direction Register	PD7	00$_{16}$
03C4$_{16}$	Port P8 Register	P8	XX$_{16}$
03C5$_{16}$	Port P9 Register	P9	XX$_{16}$
03C6$_{16}$	Port P8 Direction Register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 Direction Register	PD9	00$_{16}$
03C8$_{16}$	Port P10 Register	P10	XX$_{16}$
03C9$_{16}$			
03CA$_{16}$	Port P10 Direction Register	PD10	00$_{16}$
03CB$_{16}$	Set default value to "FF$_{16}$"		
03CC$_{16}$			
03CD$_{16}$			
03CE$_{16}$	Set default value to "FF$_{16}$"		
03CF$_{16}$	Set default value to "FF$_{16}$"		

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin package>

Address	Register	Symbol	Value after RESET
03D0₁₆			
03D1₁₆			
03D2₁₆	Set default value to "FF₁₆"		
03D3₁₆	Set default value to "FF₁₆"		
03D4₁₆			
03D5₁₆			
03D6₁₆			
03D7₁₆			
03D8₁₆			
03D9₁₆			
03DA₁₆	Pull-Up Control Register 2	PUR2	00₁₆
03DB₁₆	Pull-Up Control Register 3	PUR3	00₁₆
03DC₁₆	Set default value to "00₁₆"		
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 Register	P0	XX₁₆
03E1₁₆	Port P1 Register	P1	XX₁₆
03E2₁₆	Port P0 Direction Register	PD0	00₁₆
03E3₁₆	Port P1 Direction Register	PD1	00₁₆
03E4₁₆	Port P2 Register	P2	XX₁₆
03E5₁₆	Port P3 Register	P3	XX₁₆
03E6₁₆	Port P2 Direction Register	PD2	00₁₆
03E7₁₆	Port P3 Direction Register	PD3	00₁₆
03E8₁₆	Port P4 Register	P4	XX₁₆
03E9₁₆	Port P5 Register	P5	XX₁₆
03EA₁₆	Port P4 Direction Register	PD4	00₁₆
03EB₁₆	Port P5 Direction Register	PD5	00₁₆
03EC₁₆			
03ED₁₆			
03EE₁₆			
03EF₁₆			
03F0₁₆	Pull-up Control Register 0	PUR0	00₁₆
03F1₁₆	Pull-up Control Register 1	PUR1	XXXX 0000₂
03F2₁₆			
03F3₁₆			
03F4₁₆			
03F5₁₆			
03F6₁₆			
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆			
03FD₁₆			
03FE₁₆			
03FF₁₆	Port Control Register	PCR	XXXX XXX0₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter			Condition	Value	Unit
V_{CC}	Supply Voltage			V_{CC}=AV_{CC}	-0.3 to 6.0	V
AV_{CC}	Analog Supply Voltage			V_{CC}=AV_{CC}	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNV_{SS}, BYTE, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), V_{REF}, X_{IN}			-0.3 to V_{CC}+0.3	V
		$P7_0$, $P7_1$			-0.3 to 6.0	
V_O	Output Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{OUT}			-0.3 to V_{CC}+0.3	V
		$P7_0$, $P7_1$			-0.3 to 6.0	
Pd	Power Dissipation		T version	Topr=25° C	500	mW
			U version		400	
Topr	Operating Ambient Temperature	during CPU operation	T version		-40 to 85	° C
			U version		-40 to 105	
		during flash memory program and erase operation			0 to 60	
Tstg	Storage Temperature				-65 to 150	° C

NOTE:

1. P11 to P15 are provided in the 144-pin package only.

Table 5.2 Recommended Operating Conditions

(Vcc=4.2 to 5.5V, Vss=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version) unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
Vcc	Supply Voltage		4.2	5.0	5.5	V
AVcc	Analog Supply Voltage			Vcc		V
Vss	Supply Voltage			0		V
AVss	Analog Supply Voltage			0		V
VIH	Input High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87(3), P90-P97, P100-P107, P110-P114, P120-P127, P130-P137(4), P140-P146, P150-P157(4), XIN, RESET, CNVSS, BYTE	0.8Vcc		Vcc	V
		P70, P71	0.8Vcc		6.0	
VIL	Input Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87(3), P90-P97, P100-P107, P110-P114, P120-P127, P130-P137(4), P140-P146, P150-P157(4), XIN, RESET, CNVSS, BYTE	0		0.2Vcc	V
IOH(peak)	Peak Output High ("H") Current(2)	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(4)			-10.0	mA
IOH(avg)	Average Output High ("H") Current(1)	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(4)			-5.0	mA
IOL(peak)	Peak Output Low ("L") Current(2)	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(4)			10.0	mA
IOL(avg)	Average Output Low ("L") Current(1)	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(4)			5.0	mA

NOTES:

1. Typical values when average output current is 100 ms.
2. Total IOL(peak) for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be 80 mA or less.
   Total IOL(peak) for P3, P4, P5, P6, P7, P80 to P84, P12 and P13 must be 80 mA or less.
   Total IOH(peak) for P0, P1, P2, and P11 must be -40mA or less.
   Total IOH(peak) for P86, P87, P9, P10, P14 and P15 must be -40 mA or less.
   Total IOH(peak) for P3, P4, P5, P12 and P13 must be -40 mA or less.
   Total IOH(peak) for P6, P7, and P80 to P84 must be -40 mA or less.
3. VIH and VIL reference for P87 applies when P87 is used as a programmable input port.
   It does not apply when P87 is used as XCIN.
4. Ports P11 to P15 are provided in the 144-pin package only.

Table 5.3 Recommended Operating Conditions (Continued)

(Vcc=4.2 to 5.5V, Vss=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version) unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f(BCLK)$	CPU Operation Frequency	Vcc=4.2 to 5.5 V	0		32	MHz
$f(X_{IN})$	Main Clock Input Frequency	Vcc=4.2 to 5.5 V	0		24	MHz
$f(X_{CIN})$	Sub Clock Frequency			32.768	50	kHz
$f(Ring)$	On-chip Oscillator Frequency (Vcc=5.0V, Topr=25° C)		0.5	1	2	MHz
$f(PLL)$	PLL Clock Frequency	Vcc=4.2 to 5.5 V	10		32	MHz
$t_{SU(PLL)}$	Wait Time to Stabilize PLL Frequency Synthesizer	Vcc=5.0 V			5	ms

V_{CC}=5V

Table 5.4 Electrical Characteristics

(V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-5 mA	V_{CC}-2.0		V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-200 µA	V_{CC}-0.3		V_{CC}	V
		X_{OUT}	I_{OH}=-1 mA	3.0			V
		X_{COUT} High Power	No load applied		2.5		V
		X_{COUT} Low Power	No load applied		1.6		
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=5mA			2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=200 µA			0.45	V
		X_{OUT}	I_{OL}=1 mA			2.0	V
		X_{COUT} High Power	No load applied		0		V
		X_{COUT} Low Power	No load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN-TA4IN, TB0IN-TB5IN, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, TA0OUT-TA4OUT, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5 V			5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0 V			-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_I=0 V	30	50	167	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}			1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}			10		MΩ
V_{RAM}	RAM Standby Voltage	In stop mode		2.0			V

NOTE:

1. Ports P11 to P15 are provided in the 144-pin package only.

V_{CC}=5V

Table 5.4 Electrical Characteristics (Continued)

(V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power Supply Current	In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(BCLK)=32 MHz, Square wave, No division		28	50	mA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on ROM		430		µA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on RAM(1)		25		µA
			f(BCLK)=32 kHz, In wait mode, Topr=25° C		10		µA
			While clock stops, Topr=25° C		0.8	5	µA
			While clock stops, Topr=85° C			50	µA
			While clock stops, Topr=105° C			100	µA
			While clock stops, Topr=125° C			200	µA

NOTE:

1. Value is obtained when setting the FMSTP bit in the FMR0 register to "1" (flash memory stopped).

V_{CC}=5V

Table 5.5 A/D Conversion Characteristics

(V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	V_{REF}=V_{CC}				10	Bits
INL	Integral Nonlinearity Error	V_{REF}=V_{CC}=5V	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	V_{REF}=V_{CC}		8		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2		V_{CC}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.6 D/A Conversion Characteristics

(V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTE:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

VCC=5V

Table 5.7 Flash Memory Version Electrical Characteristics

(Vcc=4.5 to 5.5V at Topr= 0 to 60°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and Erase Endurance(2)		100			cycles
-	Word Program Time (VCC=5.0V, Topr=25° C)			25	200	µs
-	Lock Bit Program Time			25	200	µs
-	Block Erase Time (VCC=5.0V, Topr=25° C)	4-Kbyte Block		0.3	4	s
		8-Kbyte Block		0.3	4	s
		32-Kbyte Block		0.5	4	s
		64-Kbyte Block		0.8	4	s
-	All-Unlocked-Block Erase Time(1)				4 x *n*	s
tPS	Wait Time to Stabilize Flash Memory Circuit				15	µs
-	Data Hold Time (Topr=-40 to 85 ° C)		10			years

NOTES:

1. *n* denotes the number of block to be erased.
2. Number of program-erase cycles per block.
   If Program and Erase Endurance is *n* cycle (*n*=100), each block can be erased and programmed *n* cycles. For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited).

Table 5.8 Power Supply Timing

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time to Stabilize Internal Supply Voltage when Power-on	VCC=4.2 to 5.5V			2	ms

td(P-R)
Wait Time to Stabilize Internal Supply Voltage when Power-on

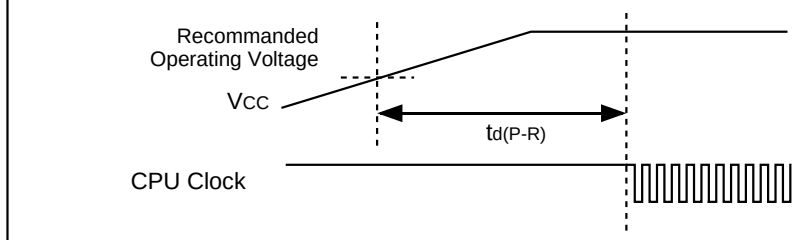


Figure 5.1 Power Supply Timing Diagram

VCC=5V

Timing Requirements

(VCC=4.2 to 5.5V, VSS=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version) unless otherwise specified)

Table 5.9 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$tw_{(H)}$	External Clock Input High ("H") Width	13.75		ns
$tw_{(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

VCC=5V

Timing Requirements

(VCC=4.2 to 5.5V, VSS=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version) unless otherwise specified)

Table 5.10 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 5.11 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 5.12 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.13 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.14 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

VCC=5V

Timing Requirements

(VCC=4.2 to 5.5V, VSS=0V at Topr = -40 to 85°C (T version)/-40 to 105°C (U version) unless otherwise specified)

Table 5.15 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on both edges)	80		ns

Table 5.16 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.17 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.18 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Pulse Width	125		ns

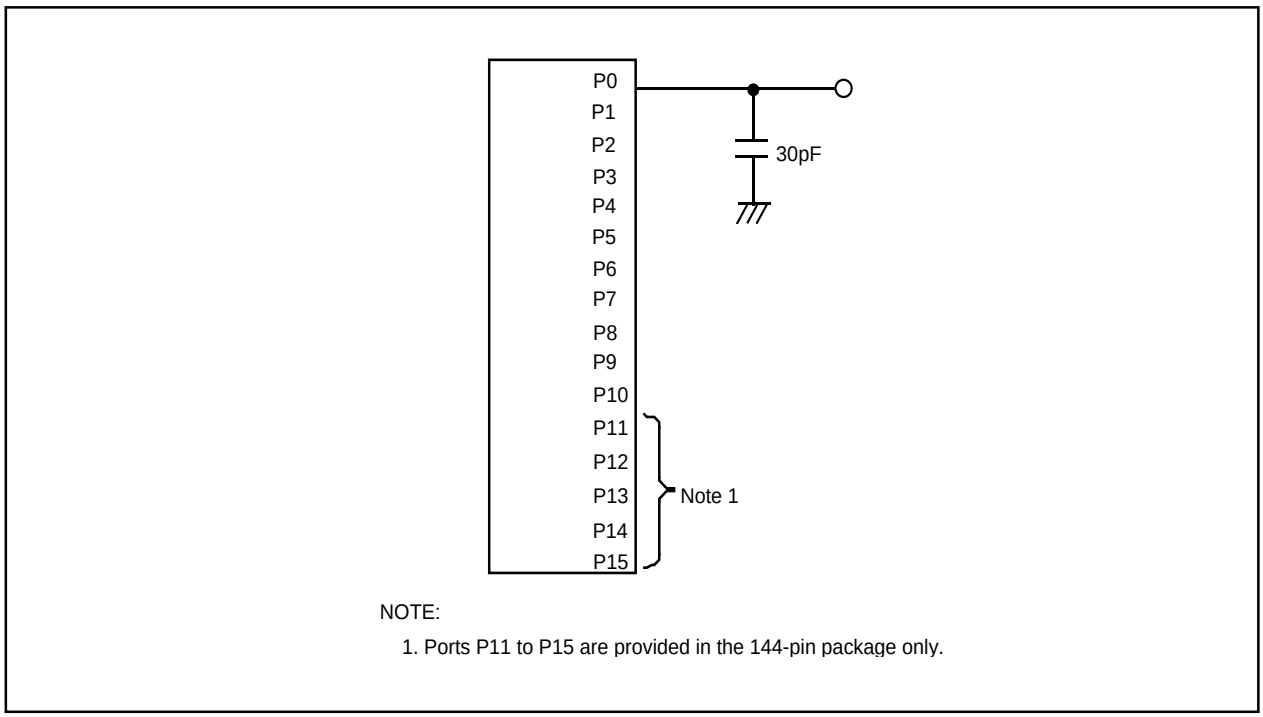
Table 5.19 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.20 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

Vcc=5V



NOTE:
1. Ports P11 to P15 are provided in the 144-pin package only.

Figure 5.2 P0 to P15 Measurement Circuit

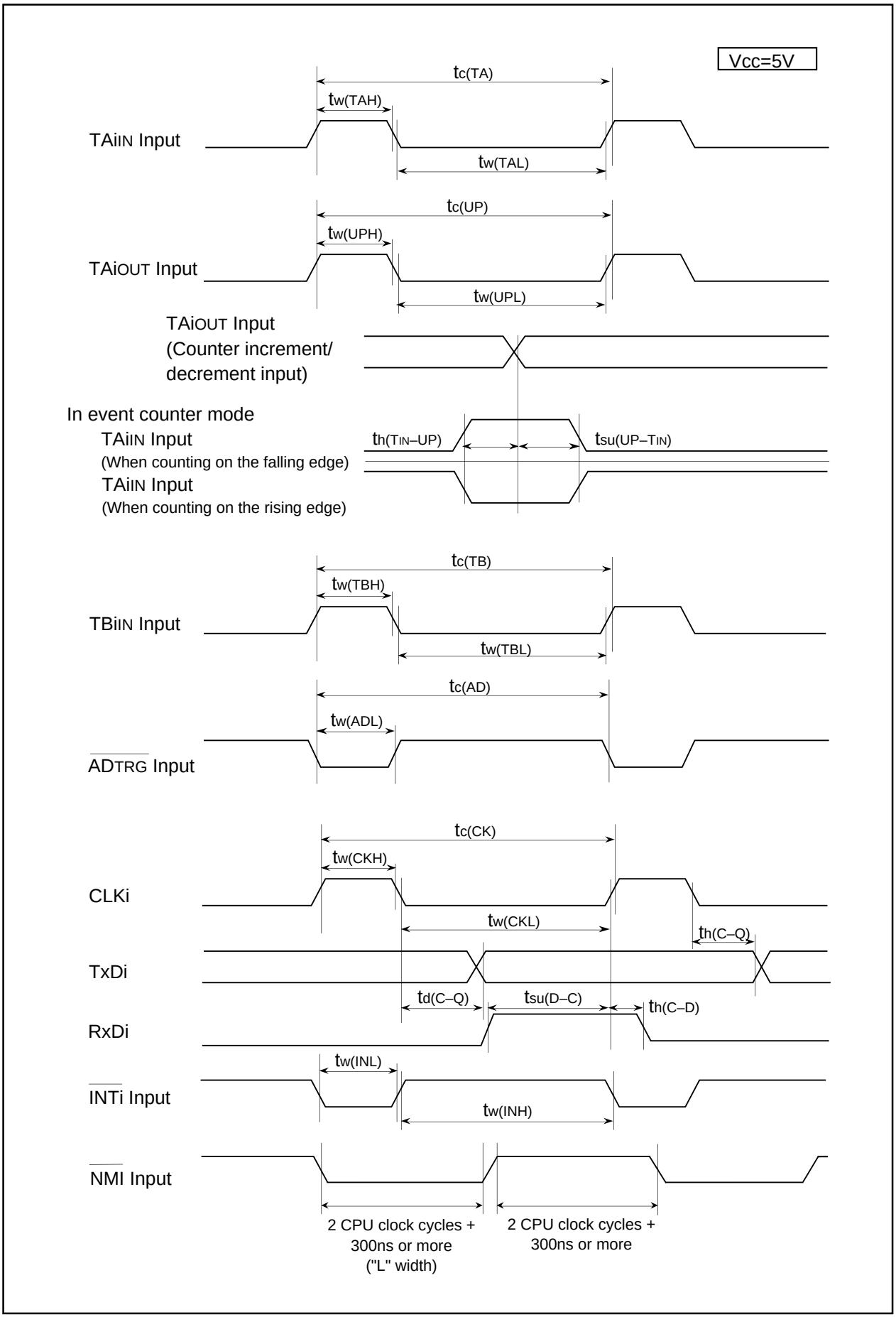
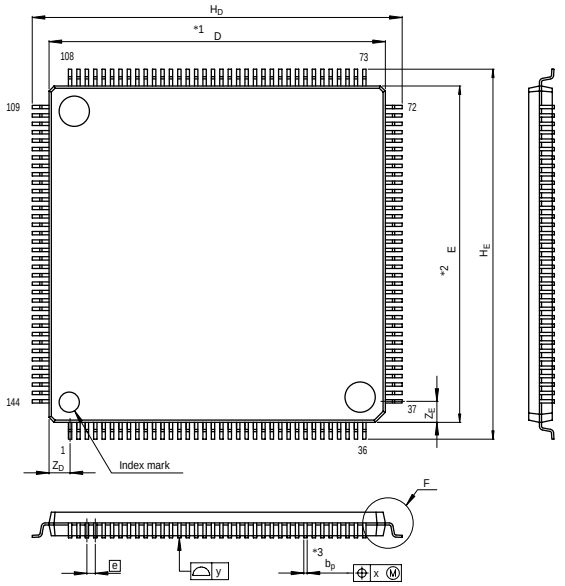
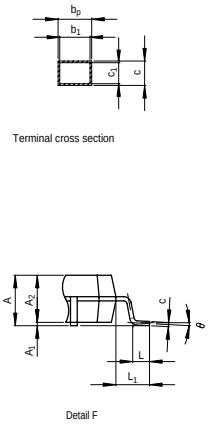


Figure 5.3 Vcc=5V Timing Diagram

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g

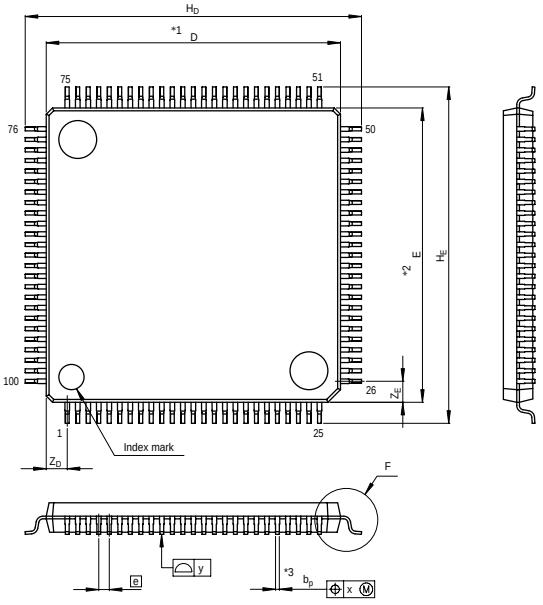


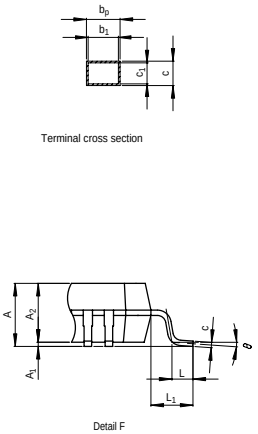


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g





NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	M32C/88 Group (M32C/88T) Datasheet

Rev.	Date	Description	
		Page	Summary
1.10	Oct.31, 2005	–	New Document

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